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# MS-7741 uATX Version: 10



## CPU:

AMD AM3r2 (HT 3.0 up to 5.2GT/s)

## System Chipset:

North Bridge : ATI RX980  
South Bridge : ATI SB950

## On Board Chip:

Super I/O : FINTEK F71808  
LAN : REALTEK RTL8111EL  
Audio Codec : REALTEK ALC887-VD2  
USB 3.0 : ASMEDIA ASM1042 \*2

## Main Memory:

Dual Channel DDRIII x 4 (Max 16GB) (1066 / 1333/ 1600 / 1866 MHz)

## Expansion Slots:

PCI-EPRESS X16 SLOT x 1  
PCI-EPRESS X 1 SLOT x 2

## PWM:

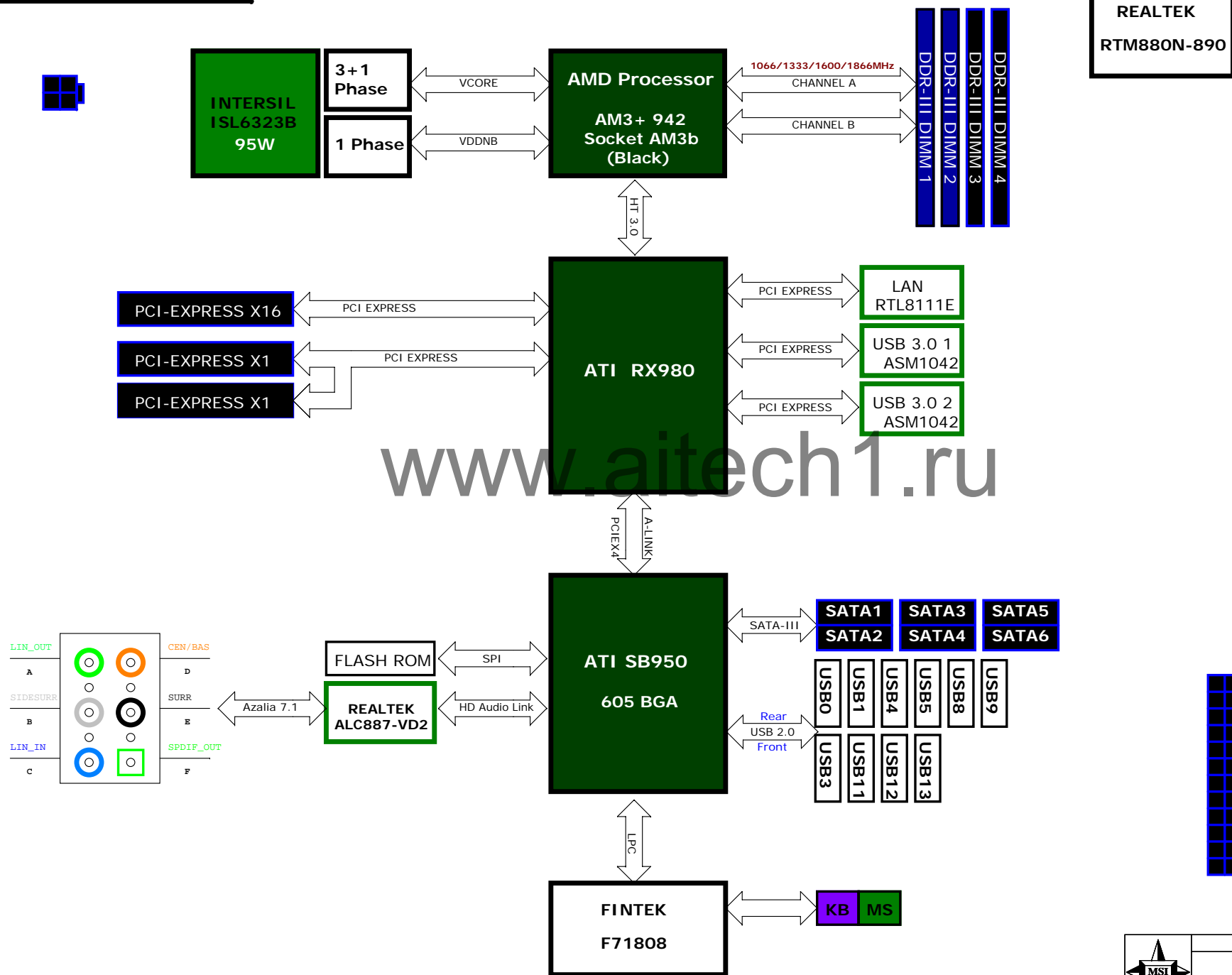
Controller : INTERSIL ISL6323B (4 Phase / 95W)

## Clock Generator:

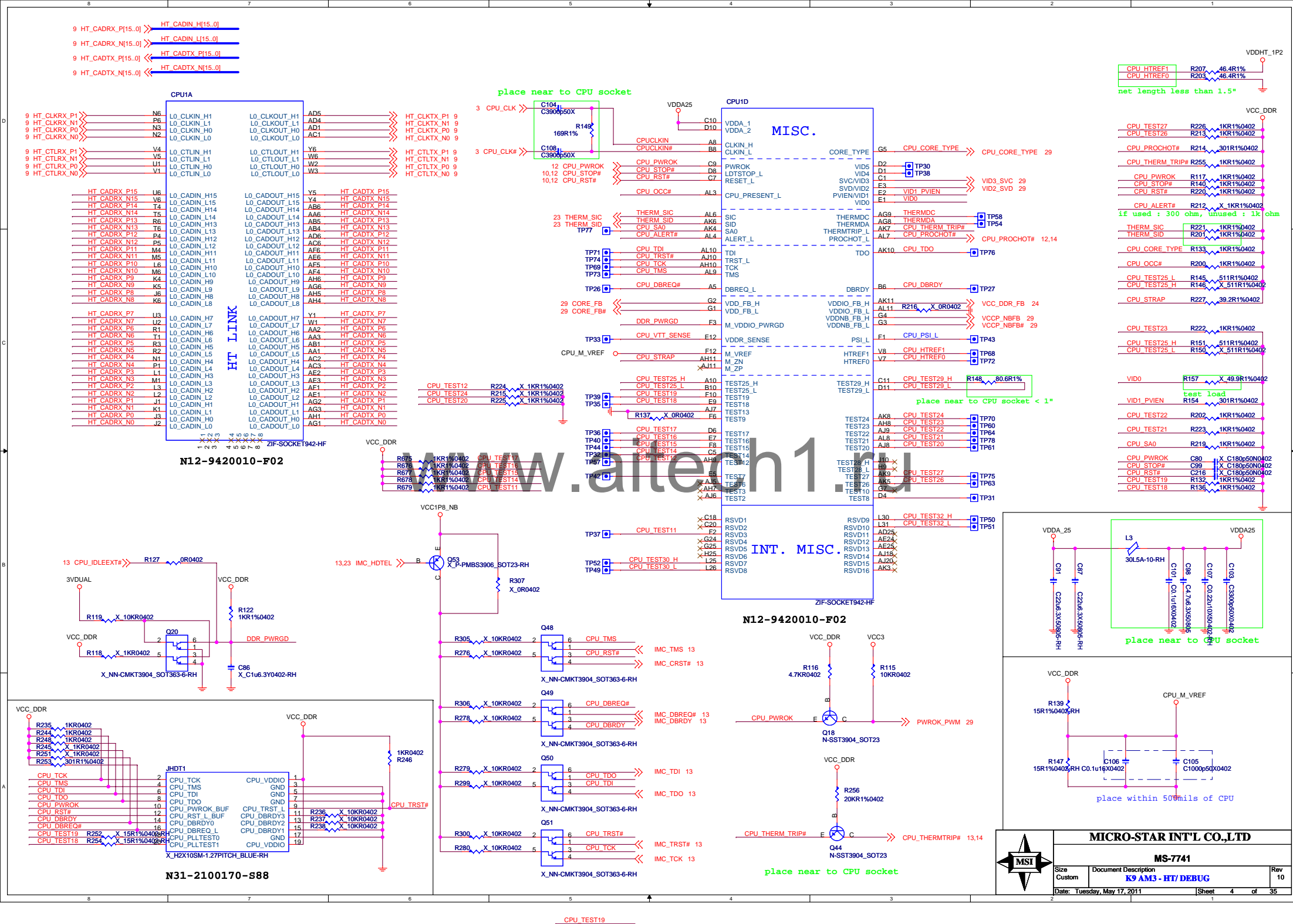
Controller : REALTEK RTM880N



# Block Diagram







7 MEM\_MA\_DQS\_N[8..0] <<<  
7 MEM\_MA\_DQS\_P[8..0] <<<  
7 MEM\_MA\_DATA[63..0] <<<  
7 MEM\_MA\_DM[7..0] <<<  
7 MEM\_MA\_ADD[15..0] <<<  
7 MEM\_MA\_CHECK[7..0] <<<

AM3

DIMM 4 MB\_CLK 5/3 MB1\_CLK 1/0  
DIMM 3 MB\_CLK 2/4 MB0\_CLK 1/0  
DIMM 2 MA\_CLK 5/3 MA1\_CLK 1/0  
DIMM 1 MA\_CLK 2/4 MA0\_CLK 1/0

DATA B

DATA A

8 MEM\_MB\_DM[7..0] <<<  
8 MEM\_MB\_ADD[15..0] <<<  
8 MEM\_MB\_CHECK[7..0] <<<  
8 MEM\_MB\_DATA[63..0] <<<  
8 MEM\_MB\_DQS\_N[8..0] <<<  
8 MEM\_MB\_DQS\_P[8..0] <<<

CPU1B

TP59 AG21 MA\_CLK\_H7  
TP56 AG20 MA\_CLK\_L7  
TP53 AE20 MA\_CLK\_H6  
TP55 AE19 MA\_CLK\_L6  
U27 U26 MA\_CLK\_H5  
V27 MA\_CLK\_H4  
W27 MA\_CLK\_L4  
W25 MA\_CLK\_H3  
U24 MA\_CLK\_H2  
V24 MA\_CLK\_L2  
G19 H19 MA\_CLK\_H1  
G20 MA\_CLK\_L1  
G21 MA\_CLK\_L0

7 MEM\_MA0\_CS#1 AC25 MA0\_CS\_L1  
7 MEM\_MA0\_CS#0 AA24 MA0\_CS\_L0  
MA0\_ODT1 AE28  
MA0\_ODT0 AC28  
7 MEM\_MA1\_CS#1 AD27 MA1\_CS\_L1  
7 MEM\_MA1\_CS#0 AA25 MA1\_CS\_L0  
MA1\_ODT1 AE27  
MA1\_ODT0 AC27  
TP45 E20 MA\_RESET\_L  
7 MEM\_MA\_CAS# AB25 MA\_CAS\_L  
7 MEM\_MA\_WE# AB27 MA\_WE\_L  
7 MEM\_MA\_RAS# AA26 MA\_RAS\_L  
7 MEM\_MA\_BANK2 N25 MA\_BANK2  
7 MEM\_MA\_BANK1 Y27 MA\_BANK1  
7 MEM\_MA\_BANK0 AA27 MA\_BANK0  
7 MEM\_MA\_CKE1 L27 MA\_CKE1  
7 MEM\_MA\_CKE0 M25 MA\_CKE0

MEM\_MA\_ADD15 M27 MA\_ADD15  
MEM\_MA\_ADD14 N24 MA\_ADD14  
MEM\_MA\_ADD13 AC26 MA\_ADD13  
MEM\_MA\_ADD12 N26 MA\_ADD12  
MEM\_MA\_ADD11 P25 MA\_ADD11  
MEM\_MA\_ADD10 Y25 MA\_ADD10  
MEM\_MA\_ADD9 N27 MA\_ADD9  
MEM\_MA\_ADD8 R24 MA\_ADD8  
MEM\_MA\_ADD7 P27 MA\_ADD7  
MEM\_MA\_ADD6 R25 MA\_ADD6  
MEM\_MA\_ADD5 R26 MA\_ADD5  
MEM\_MA\_ADD4 R27 MA\_ADD4  
MEM\_MA\_ADD3 T25 MA\_ADD3  
MEM\_MA\_ADD2 U25 MA\_ADD2  
MEM\_MA\_ADD1 T27 MA\_ADD1  
MEM\_MA\_ADD0 W24 MA\_ADD0

MEM\_MA\_DQS\_P7 AD15 MA\_DQS\_H7  
MEM\_MA\_DQS\_N7 AE15 MA\_DQS\_L7  
MEM\_MA\_DQS\_P6 AG18 MA\_DQS\_H6  
MEM\_MA\_DQS\_N6 AG19 MA\_DQS\_L6  
MEM\_MA\_DQS\_P5 AG24 MA\_DQS\_H5  
MEM\_MA\_DQS\_N5 AG25 MA\_DQS\_L5  
MEM\_MA\_DQS\_P4 AG27 MA\_DQS\_H4  
MEM\_MA\_DQS\_N4 AG28 MA\_DQS\_L4  
MEM\_MA\_DQS\_P3 C29 MA\_DQS\_H3  
MEM\_MA\_DQS\_N3 C29 MA\_DQS\_L3  
MEM\_MA\_DQS\_P2 C25 MA\_DQS\_H2  
MEM\_MA\_DQS\_N2 D25 MA\_DQS\_L2  
MEM\_MA\_DQS\_P1 F19 MA\_DQS\_H1  
MEM\_MA\_DQS\_N1 F19 MA\_DQS\_L1  
MEM\_MA\_DQS\_P0 F15 MA\_DQS\_H0  
MEM\_MA\_DQS\_N0 G15 MA\_DQS\_L0

MEM\_MA\_DM7 AF15 MA\_DM7  
MEM\_MA\_DM6 AF19 MA\_DM6  
MEM\_MA\_DM5 AJ25 MA\_DM5  
MEM\_MA\_DM4 AH29 MA\_DM4  
MEM\_MA\_DM3 B29 MA\_DM3  
MEM\_MA\_DM2 E24 MA\_DM2  
MEM\_MA\_DM1 E18 MA\_DM1  
MEM\_MA\_DM0 H15 MA\_DM0

MA\_DATA63 AE14 MEM\_MA\_DATA63  
MA\_DATA62 AG14 MEM\_MA\_DATA62  
MA\_DATA61 AG16 MEM\_MA\_DATA61  
MA\_DATA60 AD17 MEM\_MA\_DATA60  
MA\_DATA59 AD13 MEM\_MA\_DATA59  
MA\_DATA58 AE13 MEM\_MA\_DATA58  
MA\_DATA57 AG15 MEM\_MA\_DATA57  
MA\_DATA56 AE16 MEM\_MA\_DATA56  
MA\_DATA55 AG17 MEM\_MA\_DATA55  
MA\_DATA54 AE18 MEM\_MA\_DATA54  
MA\_DATA53 AD21 MEM\_MA\_DATA53  
MA\_DATA52 AG22 MEM\_MA\_DATA52  
MA\_DATA51 AE17 MEM\_MA\_DATA51  
MA\_DATA50 AE17 MEM\_MA\_DATA50  
MA\_DATA49 AF21 MEM\_MA\_DATA49  
MA\_DATA48 AE21 MEM\_MA\_DATA48  
MA\_DATA47 AF23 MEM\_MA\_DATA47  
MA\_DATA46 AE23 MEM\_MA\_DATA46  
MA\_DATA45 AJ26 MEM\_MA\_DATA45  
MA\_DATA44 AG26 MEM\_MA\_DATA44  
MA\_DATA43 AE22 MEM\_MA\_DATA43  
MA\_DATA42 AG23 MEM\_MA\_DATA42  
MA\_DATA41 AH25 MEM\_MA\_DATA41  
MA\_DATA40 AF25 MEM\_MA\_DATA40  
MA\_DATA39 AJ28 MEM\_MA\_DATA39  
MA\_DATA38 AE29 MEM\_MA\_DATA38  
MA\_DATA37 AE26 MEM\_MA\_DATA37  
MA\_DATA36 AE26 MEM\_MA\_DATA36  
MA\_DATA35 AJ27 MEM\_MA\_DATA35  
MA\_DATA34 AG29 MEM\_MA\_DATA34  
MA\_DATA33 AE27 MEM\_MA\_DATA33  
MA\_DATA32 E29 MEM\_MA\_DATA32  
MA\_DATA31 E28 MEM\_MA\_DATA31  
MA\_DATA30 E27 MEM\_MA\_DATA30  
MA\_DATA29 D27 MEM\_MA\_DATA29  
MA\_DATA28 G26 MEM\_MA\_DATA28  
MA\_DATA27 F27 MEM\_MA\_DATA27  
MA\_DATA26 C28 MEM\_MA\_DATA26  
MA\_DATA25 F25 MEM\_MA\_DATA25  
MA\_DATA24 F25 MEM\_MA\_DATA24  
MA\_DATA23 F25 MEM\_MA\_DATA23  
MA\_DATA22 E23 MEM\_MA\_DATA22  
MA\_DATA21 E23 MEM\_MA\_DATA21  
MA\_DATA20 E26 MEM\_MA\_DATA20  
MA\_DATA19 C26 MEM\_MA\_DATA19  
MA\_DATA18 G23 MEM\_MA\_DATA18  
MA\_DATA17 G23 MEM\_MA\_DATA17  
MA\_DATA16 E22 MEM\_MA\_DATA16  
MA\_DATA15 E21 MEM\_MA\_DATA15  
MA\_DATA14 F17 MEM\_MA\_DATA14  
MA\_DATA13 G17 MEM\_MA\_DATA13  
MA\_DATA12 C22 MEM\_MA\_DATA12  
MA\_DATA11 F17 MEM\_MA\_DATA11  
MA\_DATA10 G18 MEM\_MA\_DATA10  
MA\_DATA9 E17 MEM\_MA\_DATA9  
MA\_DATA8 G18 MEM\_MA\_DATA8  
MA\_DATA7 G18 MEM\_MA\_DATA7  
MA\_DATA6 G13 MEM\_MA\_DATA6  
MA\_DATA5 G13 MEM\_MA\_DATA5  
MA\_DATA4 H13 MEM\_MA\_DATA4  
MA\_DATA3 H17 MEM\_MA\_DATA3  
MA\_DATA2 E16 MEM\_MA\_DATA2  
MA\_DATA1 E14 MEM\_MA\_DATA1  
MA\_DATA0 G14 MEM\_MA\_DATA0

MA\_DQS\_H8 J28 MEM\_MA\_DQS\_P8  
MA\_DQS\_L8 J27 MEM\_MA\_DQS\_N8  
MA\_DM8 J25 MEM\_MA\_DM8  
MA\_CHECK7 K25 MEM\_MA\_CHECK7  
MA\_CHECK6 J26 MEM\_MA\_CHECK6  
MA\_CHECK5 G28 MEM\_MA\_CHECK5  
MA\_CHECK4 G27 MEM\_MA\_CHECK4  
MA\_CHECK3 L24 MEM\_MA\_CHECK3  
MA\_CHECK2 K27 MEM\_MA\_CHECK2  
MA\_CHECK1 K29 MEM\_MA\_CHECK1  
MA\_CHECK0 H27 MEM\_MA\_CHECK0

MA\_EVENT\_L W30 MEM\_MA\_EVENT# 7

1KR1%0402 R181 OVCC\_DDR  
place near to pin.

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CPU1C

TP62 AJ19 MB\_CLK\_H7  
TP67 AK19 MB\_CLK\_L7  
TP66 AL19 MB\_CLK\_H6  
TP65 AL18 MB\_CLK\_L6  
U31 MB\_CLK\_L8  
U30 MB\_CLK\_L5  
W29 MB\_CLK\_H4  
Y31 MB\_CLK\_L4  
Y31 MB\_CLK\_H3  
Y30 MB\_CLK\_L3  
V31 MB\_CLK\_H2  
V31 MB\_CLK\_L2  
A19 MB\_CLK\_H1  
C19 MB\_CLK\_L1  
D19 MB\_CLK\_H0  
MB\_CLK\_L0

8 MEM\_MB0\_CS#1 AE30 MB0\_CS\_L1  
8 MEM\_MB0\_CS#0 AC31 MB0\_CS\_L0  
MB0\_ODT1 AF31  
MB0\_ODT0 AD29  
8 MEM\_MB1\_CS#1 AE29 MB1\_CS\_L1  
8 MEM\_MB1\_CS#0 AB31 MB1\_CS\_L0  
MB1\_ODT1 AG31  
MB1\_ODT0 AD31  
8 MEM\_MB\_RESET# B19 MB\_RESET\_L  
8 MEM\_MB\_CAS# AC29 MB\_CAS\_L  
8 MEM\_MB\_WE# AC30 MB\_WE\_L  
8 MEM\_MB\_RAS# AB29 MB\_RAS\_L

8 MEM\_MB\_BANK2 E31 MB\_BANK2  
8 MEM\_MB\_BANK1 A29 MB\_BANK1  
8 MEM\_MB\_BANK0 AA28 MB\_BANK0  
MB\_CKE1 M29  
MB\_CKE0 M29

MEM\_MB\_ADD15 N28 MB\_ADD15  
MEM\_MB\_ADD14 N29 MB\_ADD14  
MEM\_MB\_ADD13 AE31 MB\_ADD13  
MEM\_MB\_ADD12 N30 MB\_ADD12  
MEM\_MB\_ADD11 P29 MB\_ADD11  
MEM\_MB\_ADD10 AA29 MB\_ADD10  
MEM\_MB\_ADD9 P31 MB\_ADD9  
MEM\_MB\_ADD8 R28 MB\_ADD8  
MEM\_MB\_ADD7 R28 MB\_ADD7  
MEM\_MB\_ADD6 R31 MB\_ADD6  
MEM\_MB\_ADD5 R30 MB\_ADD5  
MEM\_MB\_ADD4 T31 MB\_ADD4  
MEM\_MB\_ADD3 T29 MB\_ADD3  
MEM\_MB\_ADD2 U29 MB\_ADD2  
MEM\_MB\_ADD1 U28 MB\_ADD1  
MEM\_MB\_ADD0 AA30 MB\_ADD0

MEM\_MB\_DQS\_P7 AK13 MB\_DQS\_H7  
MEM\_MB\_DQS\_N7 AJ13 MB\_DQS\_L7  
MEM\_MB\_DQS\_P6 AK17 MB\_DQS\_H6  
MEM\_MB\_DQS\_N6 AJ17 MB\_DQS\_L6  
MEM\_MB\_DQS\_P5 AK23 MB\_DQS\_H5  
MEM\_MB\_DQS\_N5 AL23 MB\_DQS\_L5  
MEM\_MB\_DQS\_P4 AL28 MB\_DQS\_H4  
MEM\_MB\_DQS\_N4 AL28 MB\_DQS\_L4  
MEM\_MB\_DQS\_P3 D31 MB\_DQS\_H3  
MEM\_MB\_DQS\_N3 C31 MB\_DQS\_L3  
MEM\_MB\_DQS\_P2 C24 MB\_DQS\_H2  
MEM\_MB\_DQS\_N2 C23 MB\_DQS\_L2  
MEM\_MB\_DQS\_P1 D17 MB\_DQS\_H1  
MEM\_MB\_DQS\_N1 C17 MB\_DQS\_L1  
MEM\_MB\_DQS\_P0 C14 MB\_DQS\_H0  
MEM\_MB\_DQS\_N0 C13 MB\_DQS\_L0

MEM\_MB\_DM7 AJ14 MB\_DM7  
MEM\_MB\_DM6 AH17 MB\_DM6  
MEM\_MB\_DM5 AJ23 MB\_DM5  
MEM\_MB\_DM4 AK29 MB\_DM4  
MEM\_MB\_DM3 C30 MB\_DM3  
MEM\_MB\_DM2 A23 MB\_DM2  
MEM\_MB\_DM1 B17 MB\_DM1  
MEM\_MB\_DM0 B13 MB\_DM0

MEM\_CHB

MB\_DATA63 AH13 MEM\_MB\_DATA63  
MB\_DATA62 AL13 MEM\_MB\_DATA62  
MB\_DATA61 AL15 MEM\_MB\_DATA61  
MB\_DATA60 AJ15 MEM\_MB\_DATA60  
MB\_DATA59 AF13 MEM\_MB\_DATA59  
MB\_DATA58 AG13 MEM\_MB\_DATA58  
MB\_DATA57 AK15 MEM\_MB\_DATA57  
MB\_DATA56 AL14 MEM\_MB\_DATA56  
MB\_DATA55 AL16 MEM\_MB\_DATA55  
MB\_DATA54 AL17 MEM\_MB\_DATA54  
MB\_DATA53 AK21 MEM\_MB\_DATA53  
MB\_DATA52 AH15 MEM\_MB\_DATA52  
MB\_DATA51 AH16 MEM\_MB\_DATA51  
MB\_DATA50 AH16 MEM\_MB\_DATA50  
MB\_DATA49 AH19 MEM\_MB\_DATA49  
MB\_DATA48 AL20 MEM\_MB\_DATA48  
MB\_DATA47 AJ22 MEM\_MB\_DATA47  
MB\_DATA46 AL22 MEM\_MB\_DATA46  
MB\_DATA45 AL24 MEM\_MB\_DATA45  
MB\_DATA44 AK26 MEM\_MB\_DATA44  
MB\_DATA43 AJ21 MEM\_MB\_DATA43  
MB\_DATA42 AH21 MEM\_MB\_DATA42  
MB\_DATA41 AH23 MEM\_MB\_DATA41  
MB\_DATA40 AJ24 MEM\_MB\_DATA40  
MB\_DATA39 AL27 MEM\_MB\_DATA39  
MB\_DATA38 AL31 MEM\_MB\_DATA38  
MB\_DATA37 AG30 MEM\_MB\_DATA37  
MB\_DATA36 AL25 MEM\_MB\_DATA36  
MB\_DATA35 AL26 MEM\_MB\_DATA35  
MB\_DATA34 AJ30 MEM\_MB\_DATA34  
MB\_DATA33 AJ31 MEM\_MB\_DATA33  
MB\_DATA32 E31 MEM\_MB\_DATA32  
MB\_DATA31 E30 MEM\_MB\_DATA31  
MB\_DATA30 B29 MEM\_MB\_DATA30  
MB\_DATA29 F27 MEM\_MB\_DATA29  
MB\_DATA28 F29 MEM\_MB\_DATA28  
MB\_DATA27 F31 MEM\_MB\_DATA27  
MB\_DATA26 A29 MEM\_MB\_DATA26  
MB\_DATA25 A29 MEM\_MB\_DATA25  
MB\_DATA24 A25 MEM\_MB\_DATA24  
MB\_DATA23 A25 MEM\_MB\_DATA23  
MB\_DATA22 A24 MEM\_MB\_DATA22  
MB\_DATA21 C22 MEM\_MB\_DATA21  
MB\_DATA20 A26 MEM\_MB\_DATA20  
MB\_DATA19 B25 MEM\_MB\_DATA19  
MB\_DATA18 B23 MEM\_MB\_DATA18  
MB\_DATA17 A22 MEM\_MB\_DATA17  
MB\_DATA16 B21 MEM\_MB\_DATA16  
MB\_DATA15 A20 MEM\_MB\_DATA15  
MB\_DATA14 C16 MEM\_MB\_DATA14  
MB\_DATA13 D15 MEM\_MB\_DATA13  
MB\_DATA12 C21 MEM\_MB\_DATA12  
MB\_DATA11 A21 MEM\_MB\_DATA11  
MB\_DATA10 A17 MEM\_MB\_DATA10  
MB\_DATA9 A16 MEM\_MB\_DATA9  
MB\_DATA8 B15 MEM\_MB\_DATA8  
MB\_DATA7 A14 MEM\_MB\_DATA7  
MB\_DATA6 F13 MEM\_MB\_DATA6  
MB\_DATA5 F13 MEM\_MB\_DATA5  
MB\_DATA4 F13 MEM\_MB\_DATA4  
MB\_DATA3 G15 MEM\_MB\_DATA3  
MB\_DATA2 A15 MEM\_MB\_DATA2  
MB\_DATA1 A13 MEM\_MB\_DATA1  
MB\_DATA0 D13 MEM\_MB\_DATA0

MB0\_CS\_L1 MB0\_CS\_L0  
MB0\_ODT1 MB0\_ODT0  
MB1\_CS\_L1 MB1\_CS\_L0  
MB1\_ODT1 MB1\_ODT0  
MB\_RESET\_L  
MB\_CAS\_L MB\_WE\_L  
MB\_RAS\_L  
MB\_BANK2 MB\_BANK1  
MB\_BANK0  
MB\_CKE1 MB\_CKE0  
MB\_ADD15 MB\_ADD14  
MB\_ADD13 MB\_ADD12  
MB\_ADD11 MB\_ADD10  
MB\_ADD9 MB\_ADD8  
MB\_ADD7 MB\_ADD6  
MB\_ADD5 MB\_ADD4  
MB\_ADD3 MB\_ADD2  
MB\_ADD1 MB\_ADD0

MB\_BANK2 MB\_BANK1  
MB\_BANK0  
MB\_CKE1 MB\_CKE0  
MB\_ADD15 MB\_ADD14  
MB\_ADD13 MB\_ADD12  
MB\_ADD11 MB\_ADD10  
MB\_ADD9 MB\_ADD8  
MB\_ADD7 MB\_ADD6  
MB\_ADD5 MB\_ADD4  
MB\_ADD3 MB\_ADD2  
MB\_ADD1 MB\_ADD0

MB\_DQS\_H7 MB\_DQS\_L7  
MB\_DQS\_H6 MB\_DQS\_L6  
MB\_DQS\_H5 MB\_DQS\_L5  
MB\_DQS\_H4 MB\_DQS\_L4  
MB\_DQS\_H3 MB\_DQS\_L3  
MB\_DQS\_H2 MB\_DQS\_L2  
MB\_DQS\_H1 MB\_DQS\_L1  
MB\_DQS\_H0 MB\_DQS\_L0

MB\_DM8 J29 MEM\_MB\_DM8  
MB\_CHECK7 K29 MEM\_MB\_CHECK7  
MB\_CHECK6 K31 MEM\_MB\_CHECK6  
MB\_CHECK5 G30 MEM\_MB\_CHECK5  
MB\_CHECK4 G29 MEM\_MB\_CHECK4  
MB\_CHECK3 L29 MEM\_MB\_CHECK3  
MB\_CHECK2 L28 MEM\_MB\_CHECK2  
MB\_CHECK1 H31 MEM\_MB\_CHECK1  
MB\_CHECK0 G31 MEM\_MB\_CHECK0

MB\_EVENT\_L V29 MEM\_MB\_EVENT# 8

1KR1%0402 R180 OVCC\_DDR  
place near to pin.

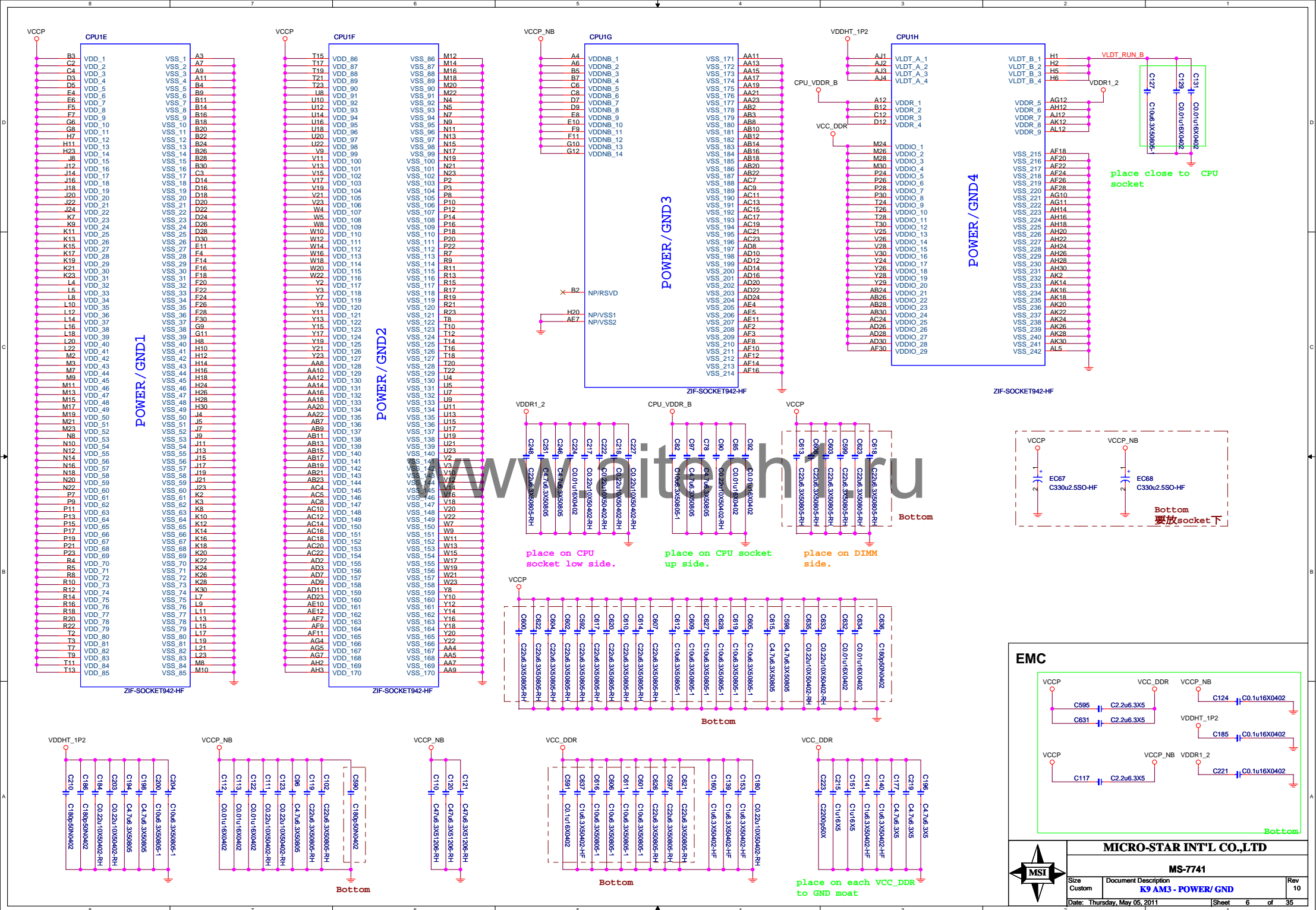
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MICRO-STAR INT'L CO.,LTD

MS-7741

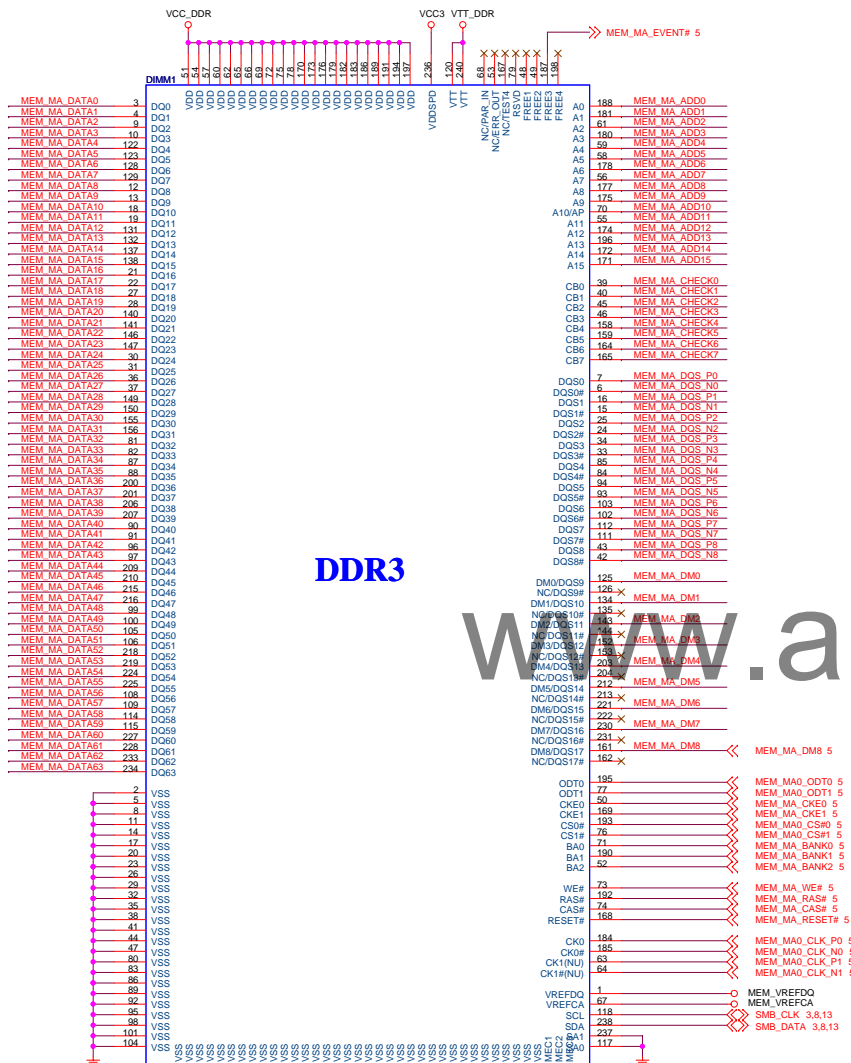
Size Custom Document Description K9 AM3 - CPU MEMORY Rev 10  
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5 MEM\_MA\_DQS\_N8\_0] MEM\_MA\_DQS\_N8\_0]  
5 MEM\_MA\_DQS\_P8\_0] MEM\_MA\_DQS\_P8\_0]  
5 MEM\_MA\_DATA63\_0] MEM\_MA\_DATA63\_0]  
5 MEM\_MA\_ADD15\_0] MEM\_MA\_ADD15\_0]  
5 MEM\_MA\_CHECK7\_0] MEM\_MA\_CHECK7\_0]  
5 MEM\_MA\_DM7\_0] MEM\_MA\_DM7\_0]

### DIMM1 / 0A

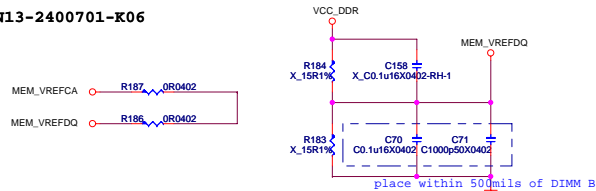


DDR3

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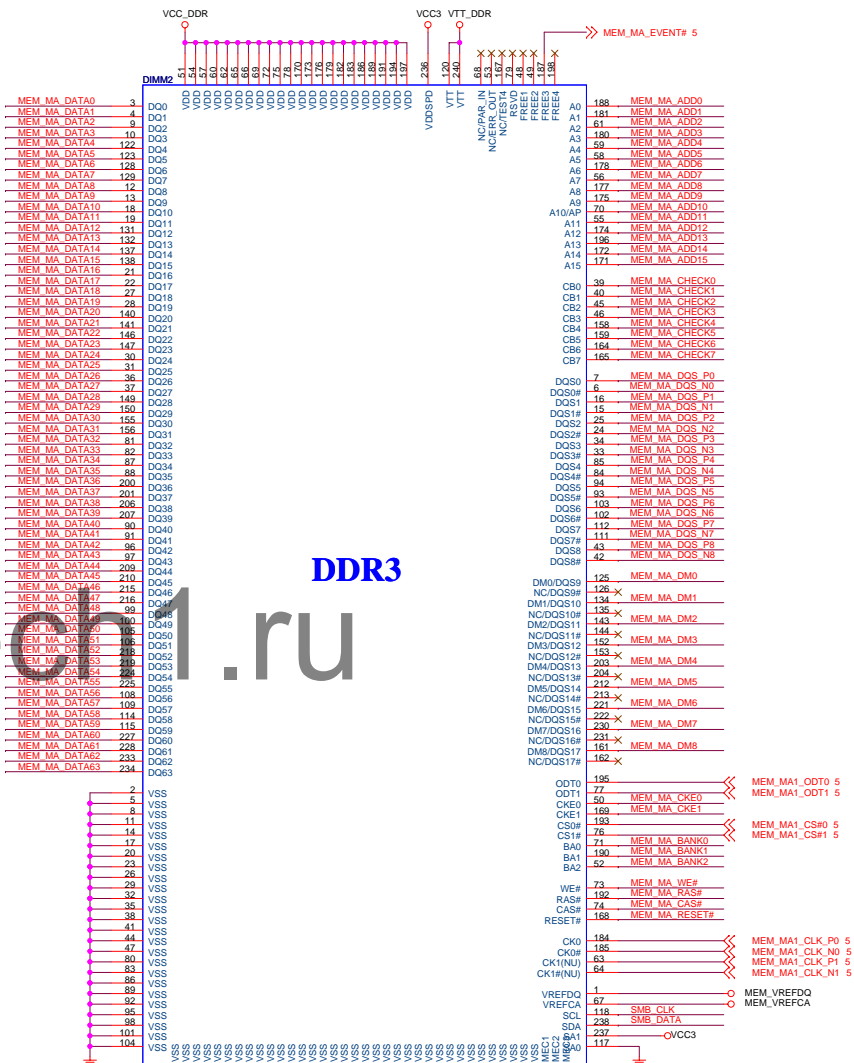
MEM\_MA\_O0T0 5  
MEM\_MA\_O0T1 5  
MEM\_MA\_CKE0 5  
MEM\_MA\_CKE1 5  
MEM\_MA\_CS#0 5  
MEM\_MA\_CS#1 5  
MEM\_MA\_BANK0 5  
MEM\_MA\_BANK1 5  
MEM\_MA\_BANK2 5  
MEM\_MA\_WE# 5  
MEM\_MA\_RAS# 5  
MEM\_MA\_CAS# 5  
MEM\_MA\_RESET# 5  
MEM\_MA\_CLK\_P0 5  
MEM\_MA\_CLK\_N0 5  
MEM\_MA\_CLK\_P1 5  
MEM\_MA\_CLK\_N1 5  
MEM\_VREFDQ  
MEM\_VREFCA  
SMB\_CLK 3.8.13  
SMB\_DATA 3.8.13

### N13-2400701-K06



MEM\_MA\_O0T0 5  
MEM\_MA\_O0T1 5  
MEM\_MA\_CKE0 5  
MEM\_MA\_CKE1 5  
MEM\_MA\_CS#0 5  
MEM\_MA\_CS#1 5  
MEM\_MA\_BANK0 5  
MEM\_MA\_BANK1 5  
MEM\_MA\_BANK2 5  
MEM\_MA\_WE# 5  
MEM\_MA\_RAS# 5  
MEM\_MA\_CAS# 5  
MEM\_MA\_RESET# 5  
MEM\_MA\_CLK\_P0 5  
MEM\_MA\_CLK\_N0 5  
MEM\_MA\_CLK\_P1 5  
MEM\_MA\_CLK\_N1 5  
MEM\_VREFDQ  
MEM\_VREFCA  
SMB\_CLK 3.8.13  
SMB\_DATA 3.8.13

### DIMM3 / 1A



DDR3



MICRO-STAR INT'L CO.,LTD			
MS-7741			
Size	Document Description	Rev	10
Custom	DDR3 - CH A DIMM 1 & 3		
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4 HT\_CADRX\_P[15..0] << HT\_CADRX\_P[15..0]  
4 HT\_CADRX\_N[15..0] << HT\_CADRX\_N[15..0]  
4 HT\_CADTX\_P[15..0] << HT\_CADTX\_P[15..0]  
4 HT\_CADTX\_N[15..0] << HT\_CADTX\_N[15..0]

U21A

PART 1/5

HT\_CADTX\_P15 T25 HT\_RXCAD15P  
HT\_CADTX\_P14 T24 HT\_RXCAD15N  
HT\_CADTX\_P13 T23 HT\_RXCAD14P  
HT\_CADTX\_P12 T22 HT\_RXCAD14N  
HT\_CADTX\_P11 T21 HT\_RXCAD13P  
HT\_CADTX\_P10 T20 HT\_RXCAD13N  
HT\_CADTX\_P9 T19 HT\_RXCAD12P  
HT\_CADTX\_P8 T18 HT\_RXCAD12N  
HT\_CADTX\_P7 T17 HT\_RXCAD11P  
HT\_CADTX\_P6 T16 HT\_RXCAD11N  
HT\_CADTX\_P5 T15 HT\_RXCAD10P  
HT\_CADTX\_P4 T14 HT\_RXCAD10N  
HT\_CADTX\_P3 T13 HT\_RXCAD9P  
HT\_CADTX\_P2 T12 HT\_RXCAD9N  
HT\_CADTX\_P1 T11 HT\_RXCAD8P  
HT\_CADTX\_P0 T10 HT\_RXCAD8N  
HT\_CADTX\_N15 T25 HT\_RXCAD7P  
HT\_CADTX\_N14 T24 HT\_RXCAD7N  
HT\_CADTX\_N13 T23 HT\_RXCAD6P  
HT\_CADTX\_N12 T22 HT\_RXCAD6N  
HT\_CADTX\_N11 T21 HT\_RXCAD5P  
HT\_CADTX\_N10 T20 HT\_RXCAD5N  
HT\_CADTX\_N9 T19 HT\_RXCAD4P  
HT\_CADTX\_N8 T18 HT\_RXCAD4N  
HT\_CADTX\_N7 T17 HT\_RXCAD3P  
HT\_CADTX\_N6 T16 HT\_RXCAD3N  
HT\_CADTX\_N5 T15 HT\_RXCAD2P  
HT\_CADTX\_N4 T14 HT\_RXCAD2N  
HT\_CADTX\_N3 T13 HT\_RXCAD1P  
HT\_CADTX\_N2 T12 HT\_RXCAD1N  
HT\_CADTX\_N1 T11 HT\_RXCAD0P  
HT\_CADTX\_N0 T10 HT\_RXCAD0N

AMD-215-0716050-RH

B01-21507Y5-A08

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The GPP lanes 6 to 9 are not supported on the RD980 and RX980, and should be left unconnected on RD980 or RX980 platforms.

21 PE\_LAN1\_RXP  
21 PE\_LAN1\_RXN  
18 PE\_USB3.01\_RXP  
18 PE\_USB3.01\_RXN  
16 GPPa\_RX4P  
16 GPPa\_RX4N  
16 GPPa\_RX5P  
16 GPPa\_RX5N  
19 PE\_USB3.02\_RXP  
19 PE\_USB3.02\_RXN

12 SB\_RXP3  
12 SB\_RXN3  
12 SB\_RXP2  
12 SB\_RXN2  
12 SB\_RXP1  
12 SB\_RXN1  
12 SB\_RXP0  
12 SB\_RXN0

VIP1\_NBPICIE  
VIP1\_NBPICIE  
VIP1\_NBPICIE  
VIP1\_NBPICIE

Spacing : 6mil

U21B

PART 2/5

16 GFX\_RX15P  
16 GFX\_RX15N  
16 GFX\_RX14P  
16 GFX\_RX14N  
16 GFX\_RX13P  
16 GFX\_RX13N  
16 GFX\_RX12P  
16 GFX\_RX12N  
16 GFX\_RX11P  
16 GFX\_RX11N  
16 GFX\_RX10P  
16 GFX\_RX10N  
16 GFX\_RX9P  
16 GFX\_RX9N  
16 GFX\_RX8P  
16 GFX\_RX8N  
16 GFX\_RX7P  
16 GFX\_RX7N  
16 GFX\_RX6P  
16 GFX\_RX6N  
16 GFX\_RX5P  
16 GFX\_RX5N  
16 GFX\_RX4P  
16 GFX\_RX4N  
16 GFX\_RX3P  
16 GFX\_RX3N  
16 GFX\_RX2P  
16 GFX\_RX2N  
16 GFX\_RX1P  
16 GFX\_RX1N  
16 GFX\_RX0P  
16 GFX\_RX0N

AC9  
AD9  
AD8  
AD7  
AC7  
AD7  
AD6  
AE6  
AF5  
AG5  
AF2  
AE1  
AD2  
AB5  
AB4  
AA6  
AA5  
Y5  
Y4  
W5  
W6  
V5  
V4  
U5  
U6  
T5  
T4  
R6  
R5  
P5  
P4

AD11  
AC11  
AE12  
AD12  
AD13  
AC13  
AE14  
AD14  
AD15  
AC15  
AE16  
AD16  
AD17  
AC17  
AD18  
AD19  
AC19  
AH20  
AG20

SB\_RX3P  
SB\_RX3N  
SB\_RX2P  
SB\_RX2N  
SB\_RX1P  
SB\_RX1N  
SB\_RX0P  
SB\_RX0N

PCE\_BCALRP  
PCE\_BCALRN  
PCE\_RCALRP  
PCE\_RCALRN  
PCE\_TCALRP  
PCE\_TCALRN

PCIE GPP1

PCIE GPP2

PCIE GPP3

PCIE ALINK

GFX\_TX15P  
GFX\_TX15N  
GFX\_TX14P  
GFX\_TX14N  
GFX\_TX13P  
GFX\_TX13N  
GFX\_TX12P  
GFX\_TX12N  
GFX\_TX11P  
GFX\_TX11N  
GFX\_TX10P  
GFX\_TX10N  
GFX\_TX9P  
GFX\_TX9N  
GFX\_TX8P  
GFX\_TX8N  
GFX\_TX7P  
GFX\_TX7N  
GFX\_TX6P  
GFX\_TX6N  
GFX\_TX5P  
GFX\_TX5N  
GFX\_TX4P  
GFX\_TX4N  
GFX\_TX3P  
GFX\_TX3N  
GFX\_TX2P  
GFX\_TX2N  
GFX\_TX1P  
GFX\_TX1N  
GFX\_TX0P  
GFX\_TX0N

AG9  
AG8  
AG7  
AG6  
AG5  
AG4  
AH4  
AE3  
AC3  
AC2  
AB2  
AB1  
AA2  
Y2  
V2  
W2  
U2  
T2  
R2  
P2  
P1

GPP\_TX9P  
GPP\_TX9N  
GPP\_TX8P  
GPP\_TX8N  
GPP\_TX7P  
GPP\_TX7N  
GPP\_TX6P  
GPP\_TX6N  
GPP\_TX5P  
GPP\_TX5N  
GPP\_TX4P  
GPP\_TX4N  
GPP\_TX3P  
GPP\_TX3N  
GPP\_TX2P  
GPP\_TX2N  
GPP\_TX1P  
GPP\_TX1N  
GPP\_TX0P  
GPP\_TX0N

SB\_TX3P  
SB\_TX3N  
SB\_TX2P  
SB\_TX2N  
SB\_TX1P  
SB\_TX1N  
SB\_TX0P  
SB\_TX0N

PCE\_BCALRP  
PCE\_BCALRN  
PCE\_RCALRP  
PCE\_RCALRN  
PCE\_TCALRP  
PCE\_TCALRN


The GFX2 lanes are not supported on the RD980 and RX980, and should be left unconnected on RD980 or RX980 platforms.

The GPP lanes 6 to 9 are not supported on the RD980 and RX980, and should be left unconnected on RD980 or RX980 platforms.

PE\_LAN1\_TXPC  
PE\_LAN1\_TXNC  
PE\_USB3.01\_TXPC  
PE\_USB3.01\_TXNC  
GPPa\_TX4P  
GPPa\_TX4N  
GPPa\_TX5P  
GPPa\_TX5N  
PE\_USB3.02\_TXPC  
PE\_USB3.02\_TXNC

SB\_TXP3  
SB\_TXN3  
SB\_TXP2  
SB\_TXN2  
SB\_TXP1  
SB\_TXN1  
SB\_TXP0  
SB\_TXN0

PCE\_BCALRP  
PCE\_BCALRN  
PCE\_RCALRP  
PCE\_RCALRN  
PCE\_TCALRP  
PCE\_TCALRN



**MICRO-STAR INT'L CO.,LTD**

**MS-7741**

Size Custom Document Description **RD890 - HT LINK/ PCIE I / F** Rev 10

Date: Monday, May 16, 2011 Sheet 9 of 35

#### DFT\_GPIO5: STRAP\_DEBUG\_BUS\_GPIO\_ENABLED

Enables the Test Debug Bus using GPIO.  
1 : Disable ( Can still be enabled using nbcfg register access)  
0 : Enable

#### DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.  
GPIO4:3:2

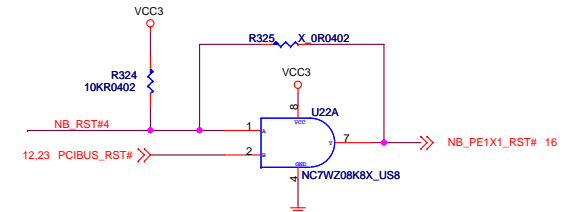
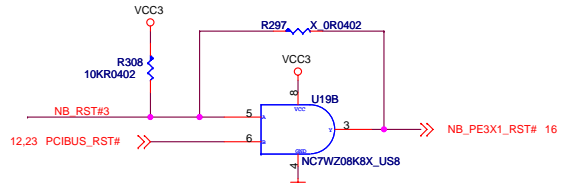
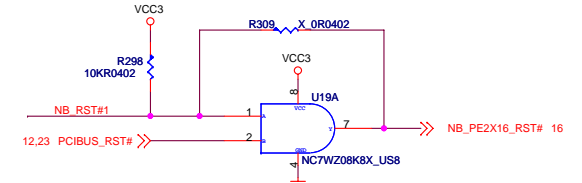
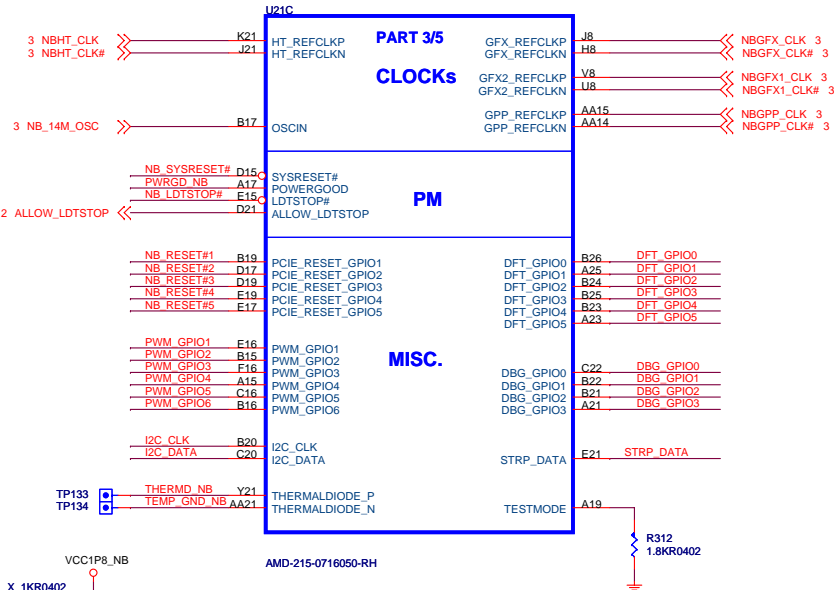
010 : 1:1:1:1:1:1:4 L

#### DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

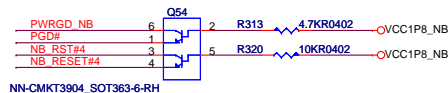
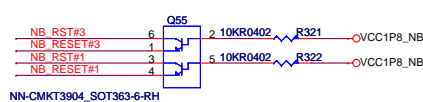
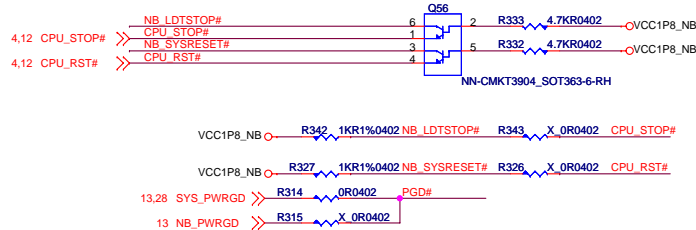
Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EPROM if connected, or use default values if not connected

#### DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLED

Enables the Test Debug Bus using PCIE bus  
1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable



T70-7WZ0800-F01

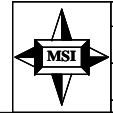




PLACE PCIE CAPS  
CLOSE TO SB850

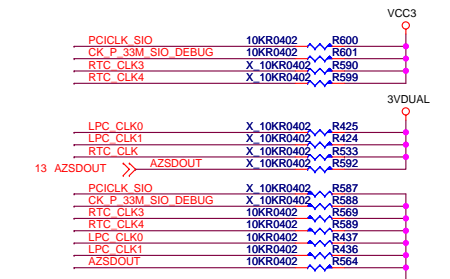
N91-01F0151-H06

N41-1030141-H06  
N31-1030151-N33-1020271-RH

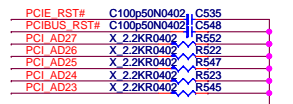


MICRO-STAR INT'L CO.,LTD		
MS-7741		
Size	Document Description	Rev
Custom	SB850 - PCIE/PCI/CPU/LPC	10
Date:	Monday, May 16, 2011	Sheet 12 of 35

## REQUIRED STRAPS



	PULL HIGH	PULL LOW
PCICLK1	Allow PCIE	Force PCIE Gen 1
PCICLK2	Watchdog timer on NB_PWGRD Enabled	Watchdog timer on NB_PWGRD Disabled
PCICLK3	Denug Straps Enabled	Denug
PCICLK4	NON-FUSION	FUSION CLOCK MODE
LPC_CLK0	CLOCK MODE	DISABLED EC
LPC_CLK1	CLK GEN ENABLE	DISABLED
AZSDOUT	LOW PWR MODE	PERF MODE



## DEBUG STRAPS

	PULL HIGH	PULL LOW
PCI_AD27	USE PCI	BYPASS PCI PLL
PCI_AD26	DISABLE ILA	ENABLE ILA AUTORUN
PCI_AD25	USE FC	BYPASS FC PLL
PCI_AD24	USE DEFAULT	USE EEPROM PCIE STRAPS
PCI_AD23	DISABLE PCIE MEM_BOOT	ENABLE PCIE MEM_BOOT

Place crystal close to SB750,  
and use GND guard for net.

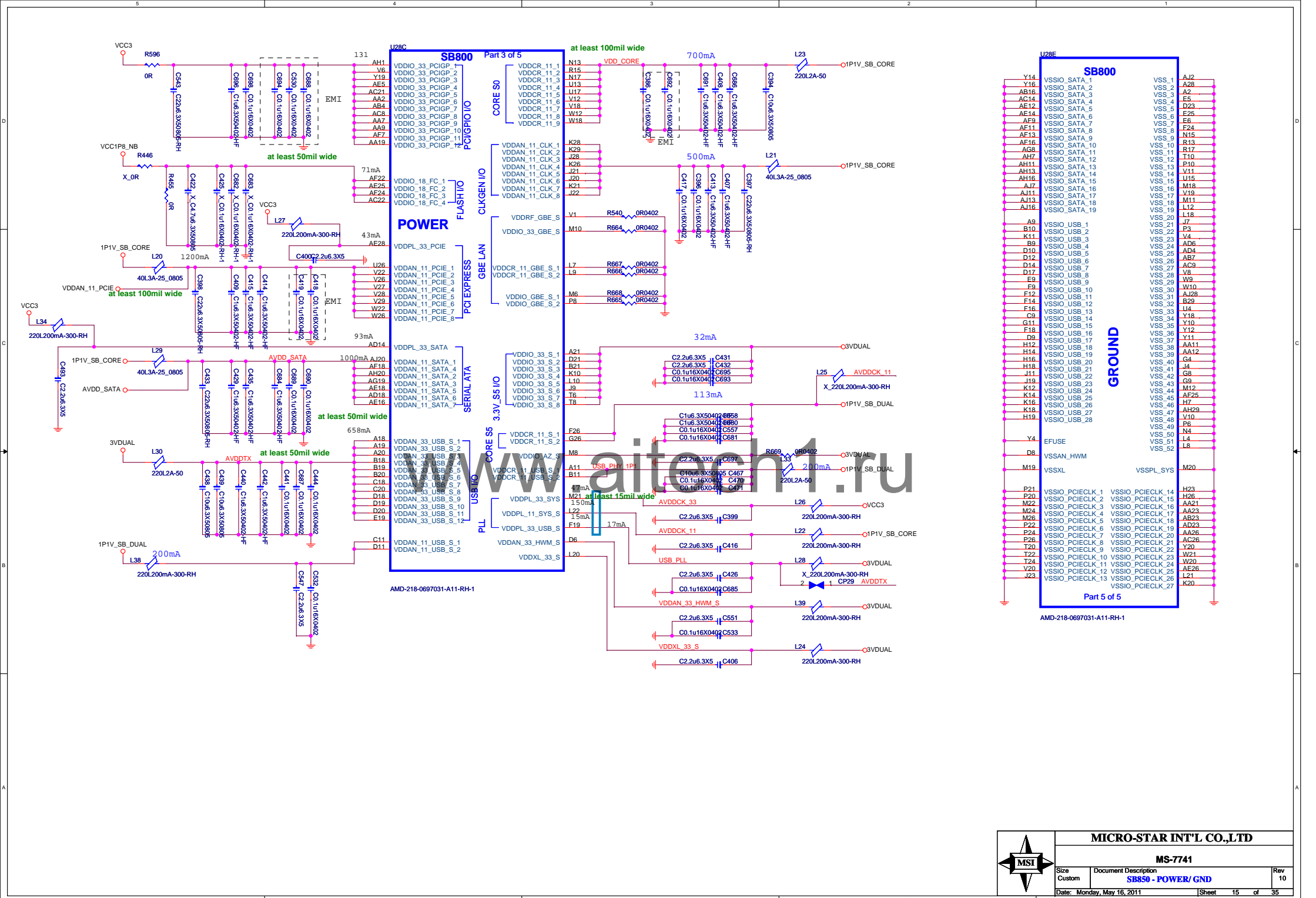
D04-0300200-C11

www.aitech1.ru

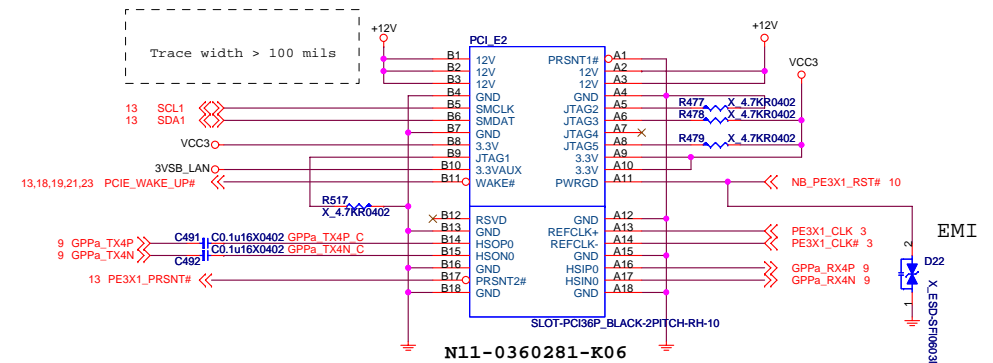
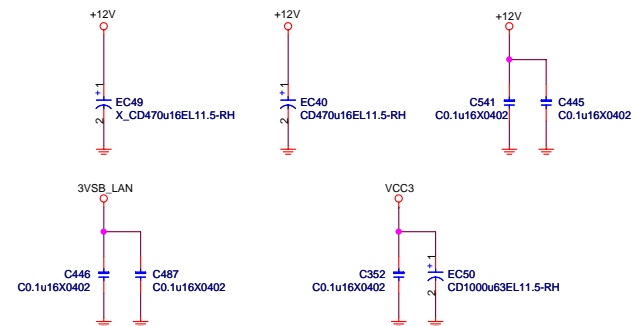








PCI-EXPRESS X1

[illegible]

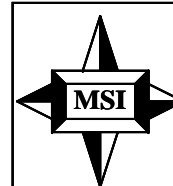
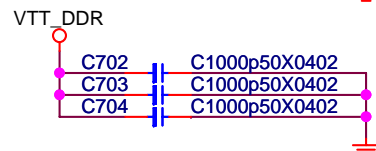
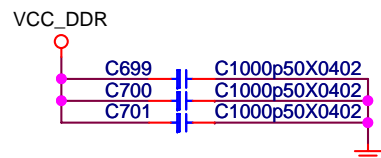
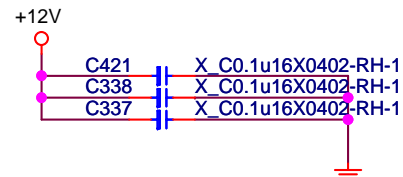
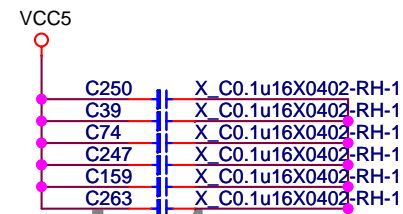
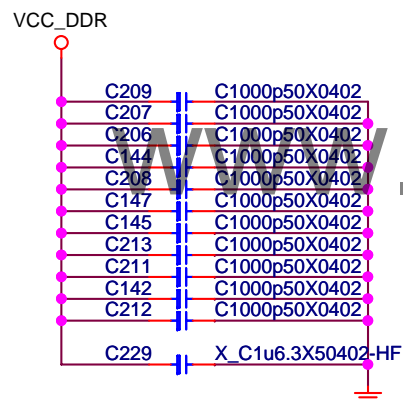
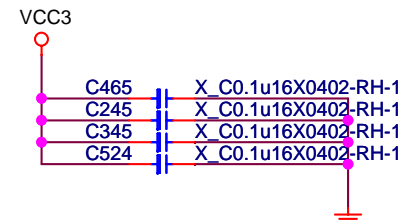
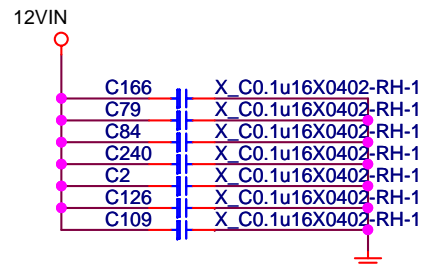
記得在SLOT旁接電容



MS-7741

Size Custom	Document Description <b>PE_X1Slot 1,3 &amp; PE_X16 Slot 2</b>	Rev 10
Date: Monday, May 16, 2011		Sheet 16 of 35

# EMI



**MICRO-STAR INT'L CO.,LTD**

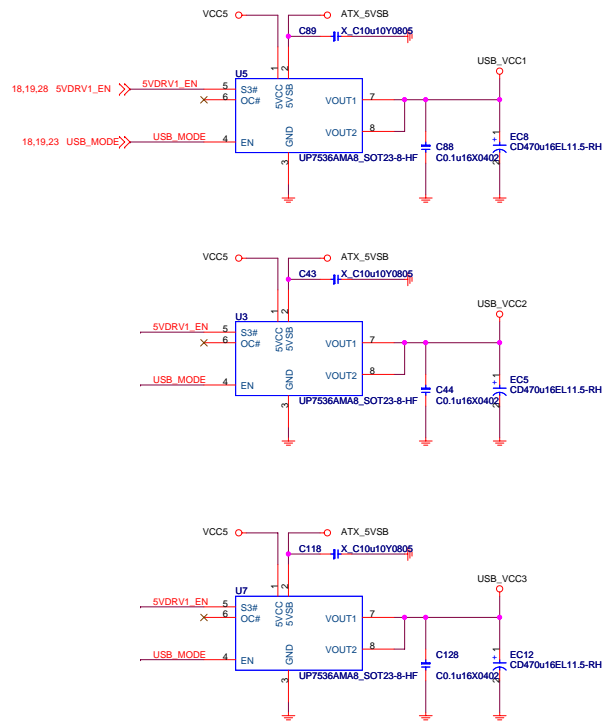
**MS-7741**

Size	Document Description	Rev
A	<b>EMI Solution</b>	10
Date: Thursday, May 05, 2011		Sheet 17 of 35

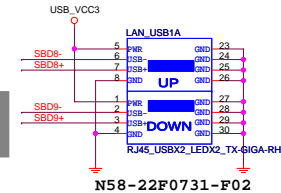
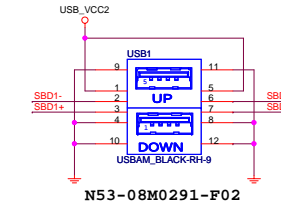
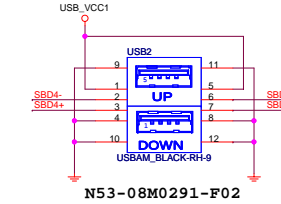
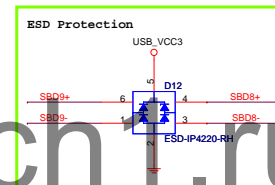
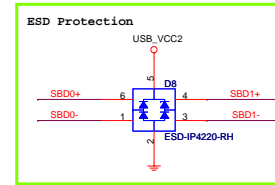
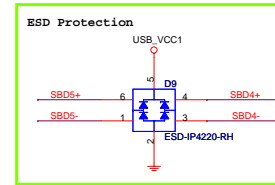
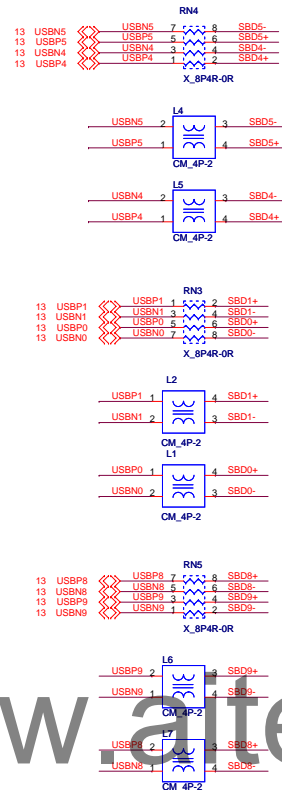




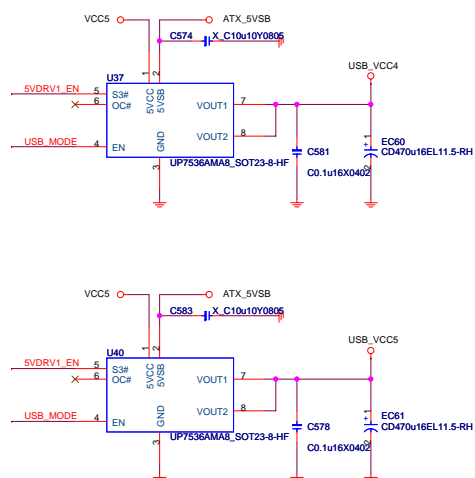
## POWER CIRCUIT FOR USB PORT 0,1



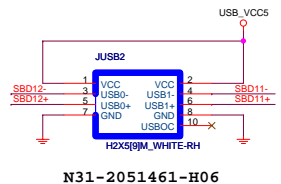
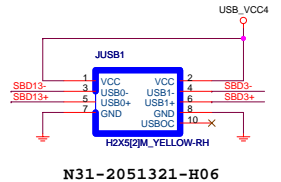
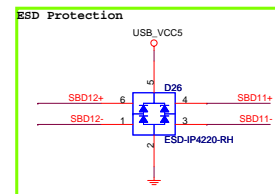
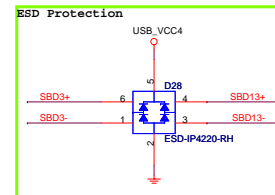
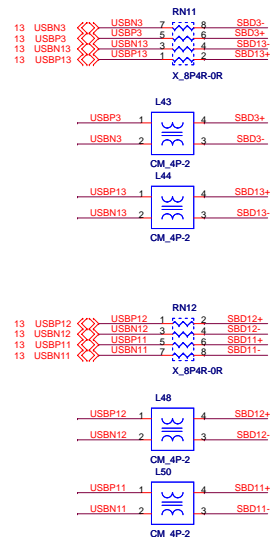
## REAR PANEL USB CONNECTOR FOR USB PORT 0 ~ 7



## POWER CIRCUIT FOR USB PORT 8,9,10



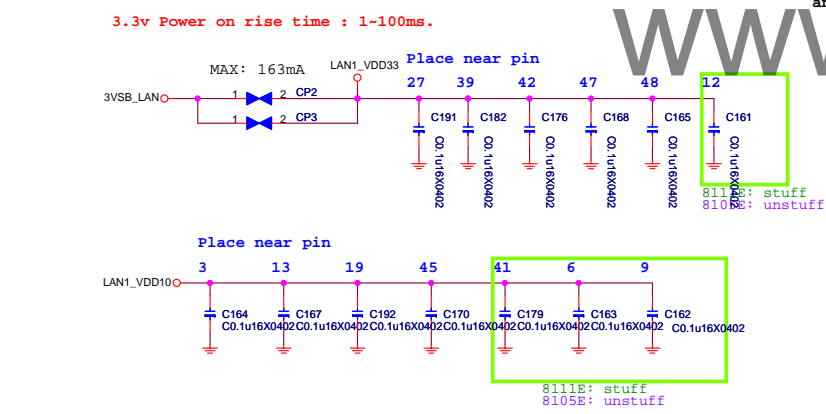
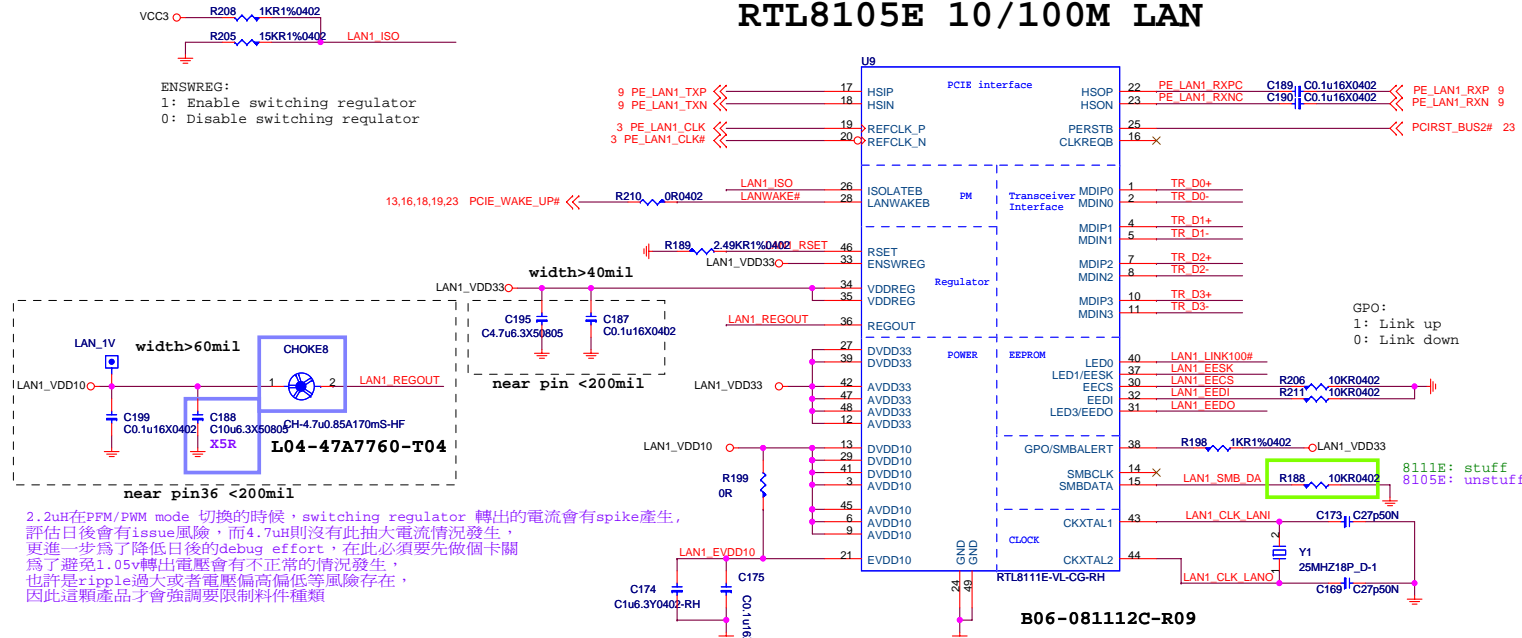
## FRONT PANEL USB CONNECTOR FOR USB PORT 8 ~ 11





# RTL8111E Giga LAN

# RTL8105E 10/100M LAN



8105E POWER Consumption

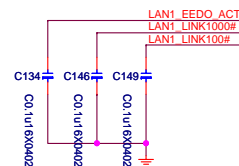
	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

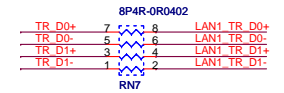
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

R14, R15, R17請依據所使用的LAN connector上的LED亮度去調整阻值

only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM



Remove pull-up R if R existence on motherboard (or SB has internal pull-up R).

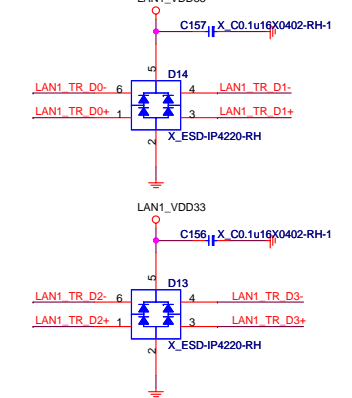


Near Lan Chip



Near Lan Chip

## Reserve ESD Protect NEAR CONNECTOR



1pF D0G-0422003-P03  
2pF D0G-0200529-A68  
D0G-0422003-N47  
D0G-0303309-C12

Giga-Lan	10/100-Lan
N58-22F0731-F02	N58-22F0061-F02
N58-22F0731-S42	N58-22F0061-F02
N58-22F0731-I60	N58-22F0061-F02
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	100 Green
100 Green	10 None
10 None	10 None
19 Yellow	19 Yellow
20 Yellow	20 Yellow
21 Orange	21 Green
22 Green	22 Green



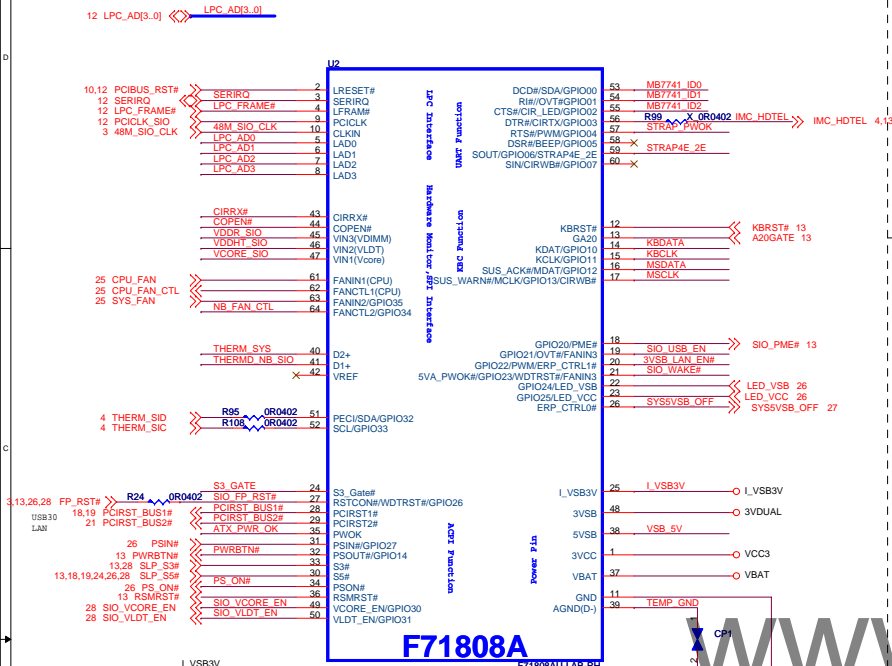
## MICRO-STAR INT'L CO.,LTD

MS-7741

Size	Document Description	Rev
Custom	LANI RTL 8111E	10
Date: Monday, May 16, 2011	Sheet 21 of 35	

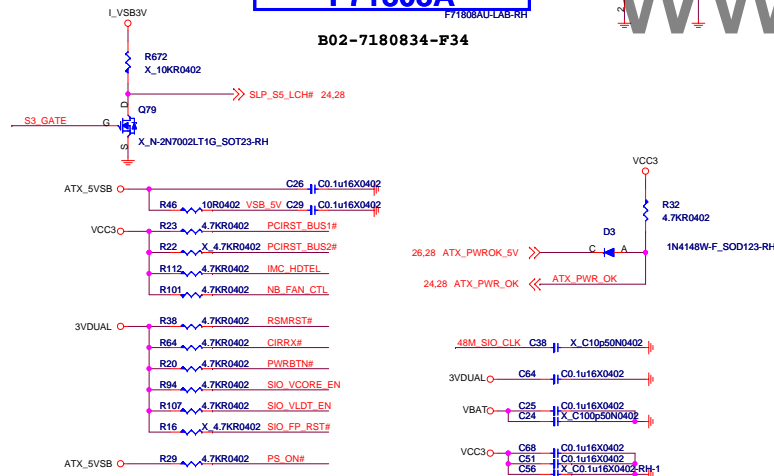


## LPC SUPER I/O F71889AD



F71808A

B02-7180834-F34



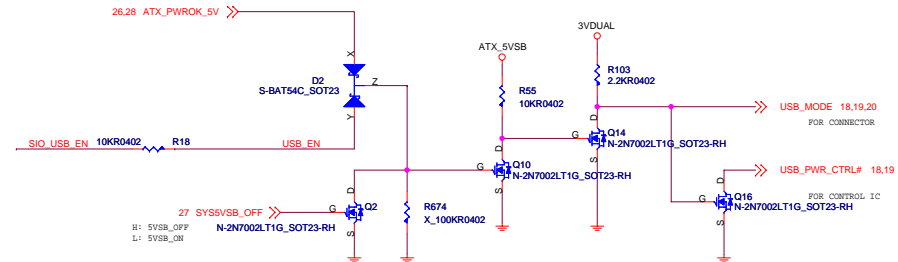
## LPC I/O STRAPPING RESISTOR

POWER-ON TRIP

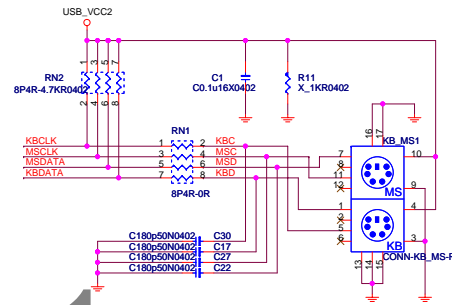
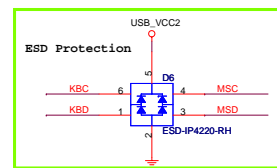


PIN	Function	NET Name	HI	LO
59	Config 4E/2E	SOUTA	4E	2E
57	STRAP_PWOK	STRAP_PWOK	PWOK (pin 35) for AMD	PWOK (pin 35) for Intel

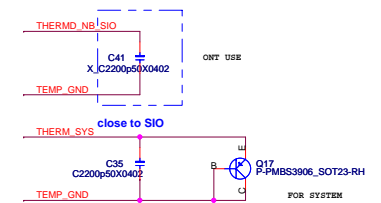
## USB MODE CONTROL



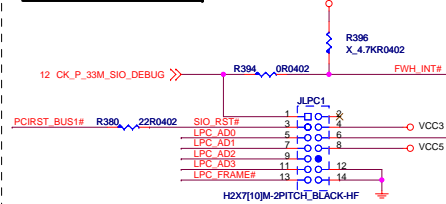
## Keyboard / Mouse PS2 CONNECT



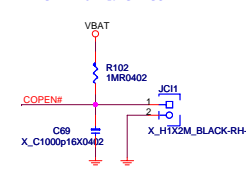
N56-12F0081-F02

Temperature Sensing  
Diode / Resistor SENSING CIRCUIT

## LPC Debug Port



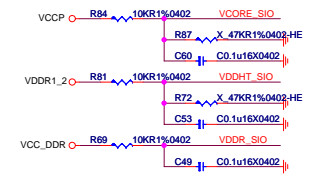
N31-2071271-H06

Chassis Intrusion  
CASE OPEN CIRCUIT

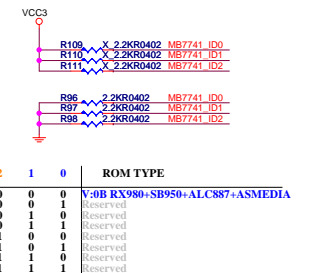
N31-1020211-H06

## VOLTAGE SENSING (H/W Monitor)

The best voltage input level is about 1V.

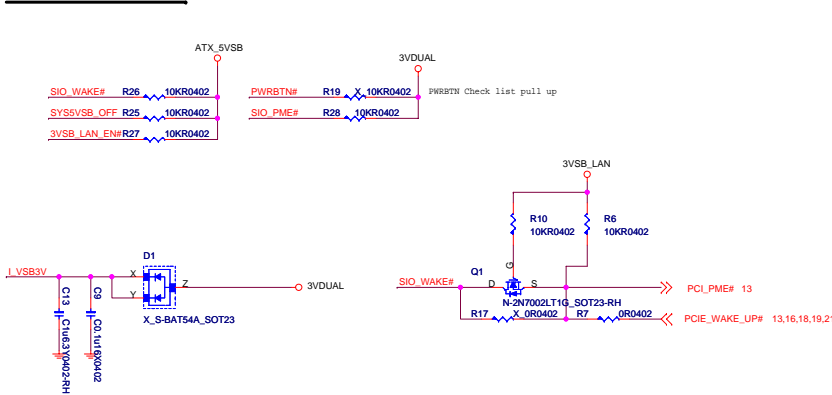


## MS-7741 SKU CONTROL



ROM TYPE		
2	1	0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

## F71889EF EUP Function



MICRO-STAR INT'L CO.,LTD

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1.5V@25.7A

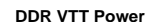


S0 / S1 For NB VDDHTRX 1.1V

For NB VDDC 1.1V

For NB NBPCIE 1.1V

For NB VDDHTRX 1.1V



---

0.75V@2A

To CPU Copper trace width > 250mils , Fill  
island behind DIMM > 400mils .

$$0.2075A \cdot 6 = 1.245A$$


**MICRO-STAR INT'L CO.,LTD**

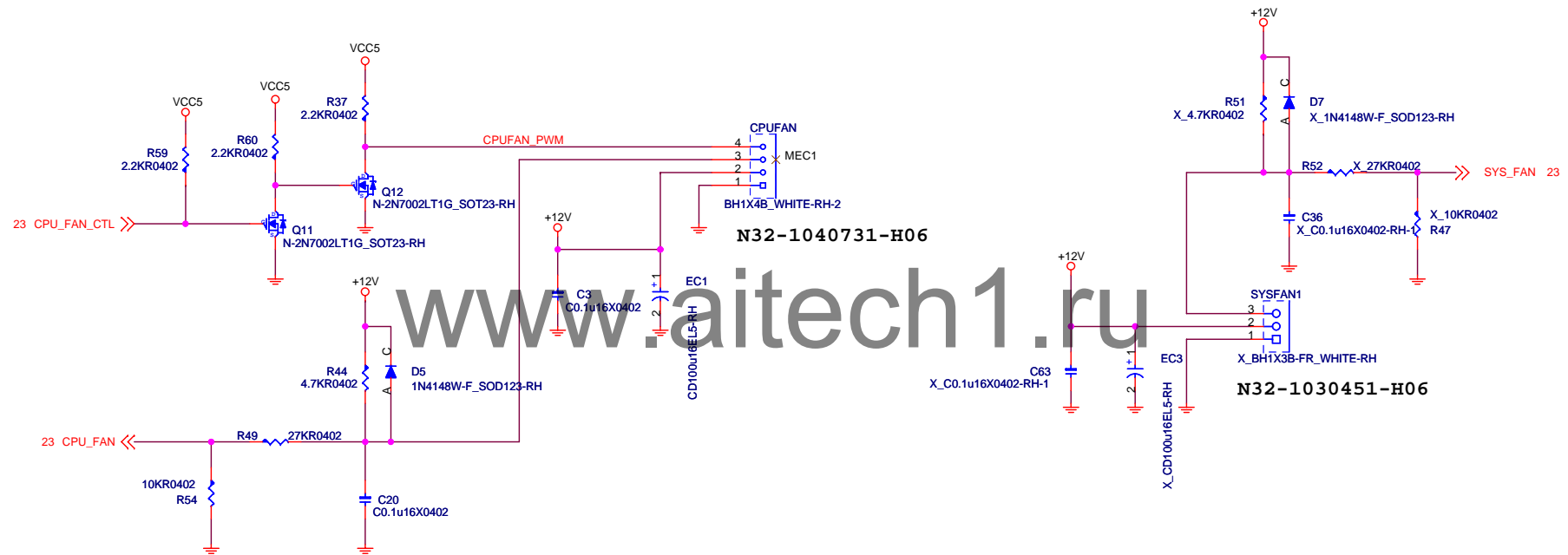
MS-7741

Size	Document Description
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C	<b>DDR &amp; NBCORE_POWER</b>		
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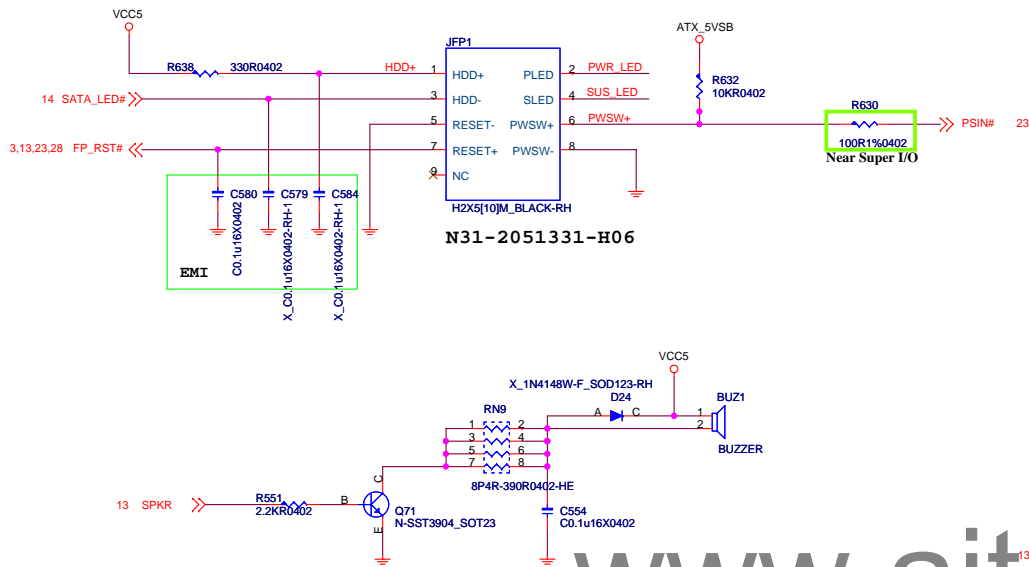
## CPU FAN

## SYS FAN

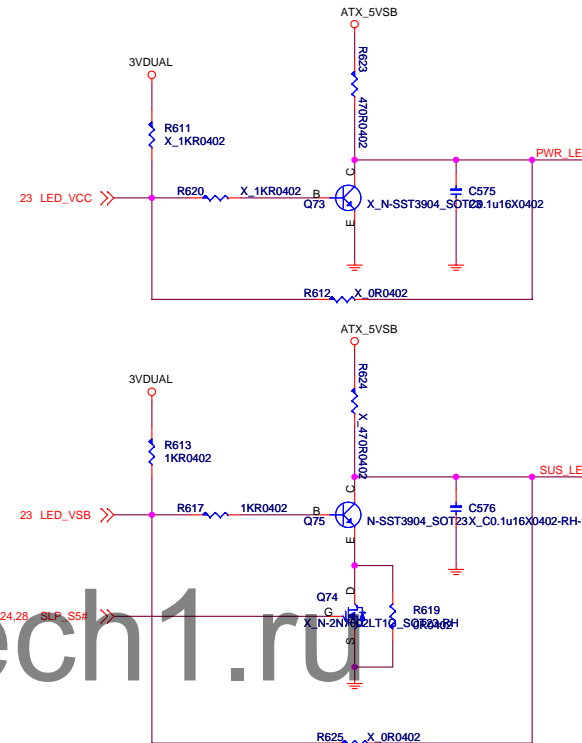


# ATX connector / Front Panel

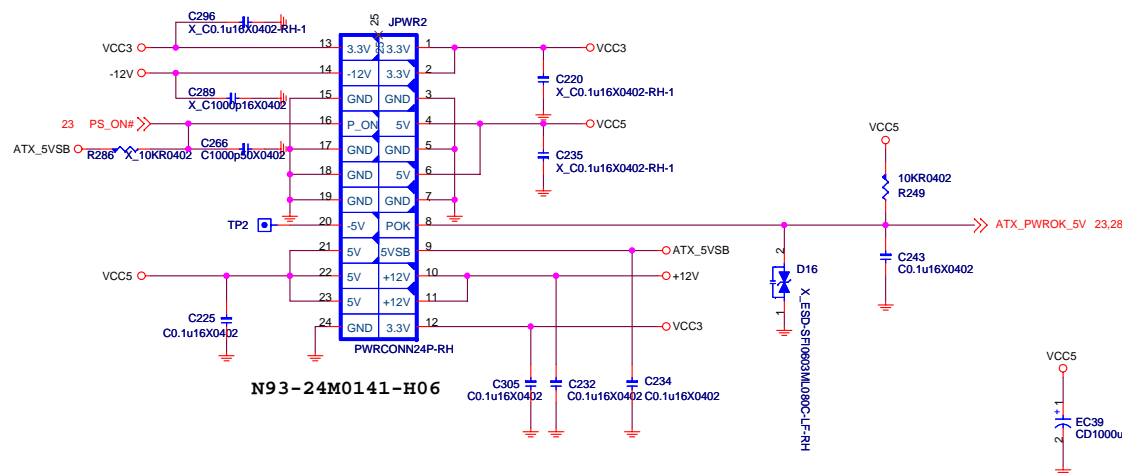
## Intel Front Panel



## LED ( for Fintek 71889)



## ATX Power Connector (2x12)

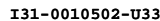


MICRO-STAR INT'L CO.,LTD		
MS-7741		
Size	Document Description	Rev
Custom	ATX / Front Panel / LED	10
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```
Vout : 0.8 [ ( R593+R599 ) / R599 ] = 3.3 Volt
Vout : 0.8 [ ( 10K+3.3K ) / 3.3K ] = 3.22 Volt

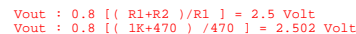
For SB USB 1.2V, 310mA
For SB 3VDUAL 3.3V, 712mA
```



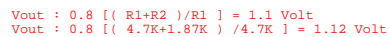
For NR IDD: 1.8u



## up7707: 600mA Low Dropout Linear Regulator



For SB VDD 1.1V



For CPU VDDR 1.2V	4A
For CPU VLDT 1.2V	2.5A
For NB VDDHTTX 1.2V	1A



ATX\_5VSB

R233 X\_OR

R234 X\_OR

R239 X\_OR

Trace Width 80mils.

ATX\_5VSB

VCC5\_SB

C236 C1u16X5

C241 10KR

C706 C1u16X5

Q43 P-P06P03LDG\_TO252-RH

VCC5\_SB

EC26 CD100u16EL5-RH

DSW\_3VSB

3VDUAL

3VDUAL

3VDUAL

EC41 X\_CD100u16EL5-RH

C459 C10u6.3X50805

1.1A(S0)

DSW\_3VSB

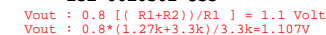
3VSB\_LAN

3VSB\_LAN

3VSB\_LAN

EC62 X\_CD100u16EL5-RH

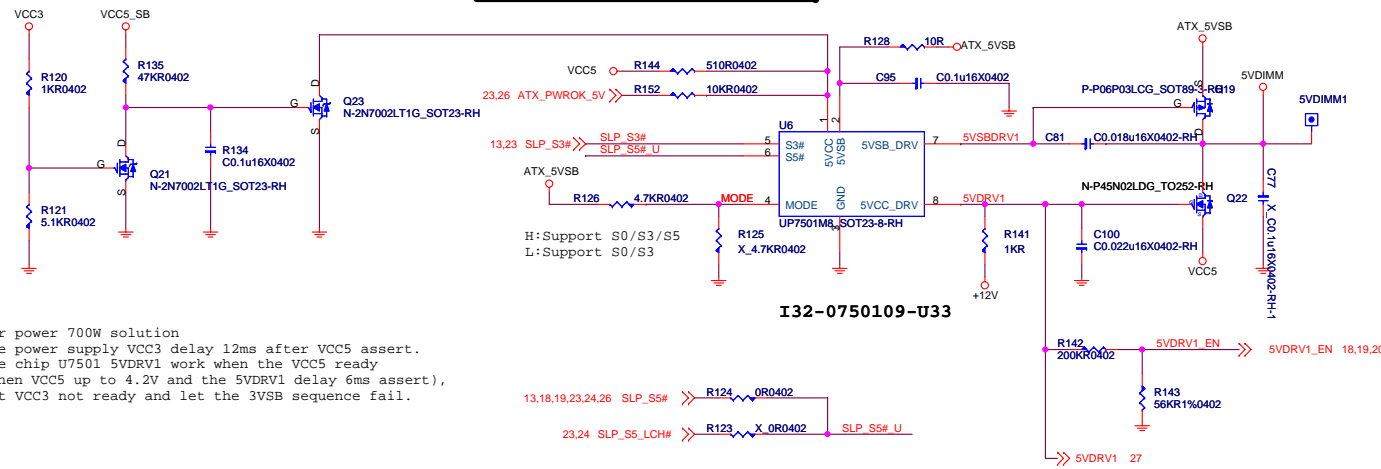
3VDUAL 1.1W



MS-7741

Size Custom	Document Description <b>SYS_POWER_LDO/ Regulator</b>	Rev 10
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## 5VDIMM FOR DDR



For power 700W solution  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert),  
but VCC3 not ready and let the 3VSB sequence fail.

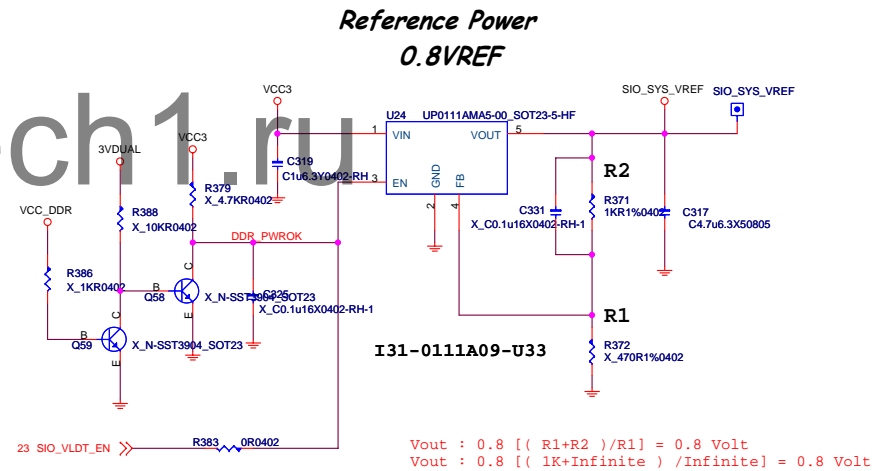
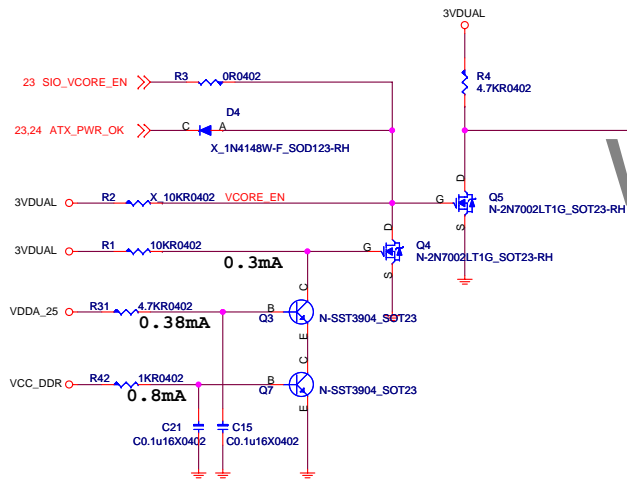
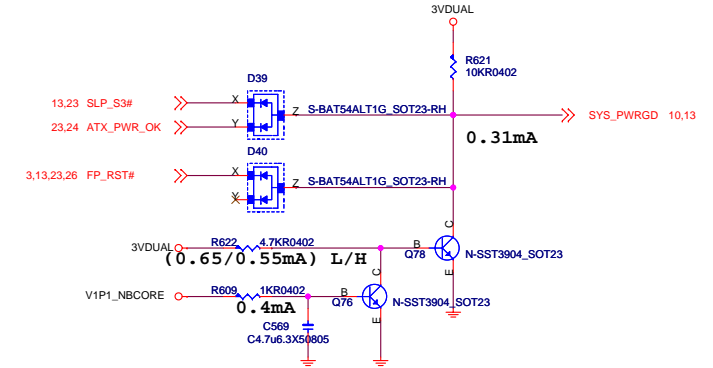


Table 34. DDR3 Power Sequencing Group Definitions

Power Group A	Power Group B
VDDIO	VDD
VDDA	VDDNB
	VLDI
	VDDR



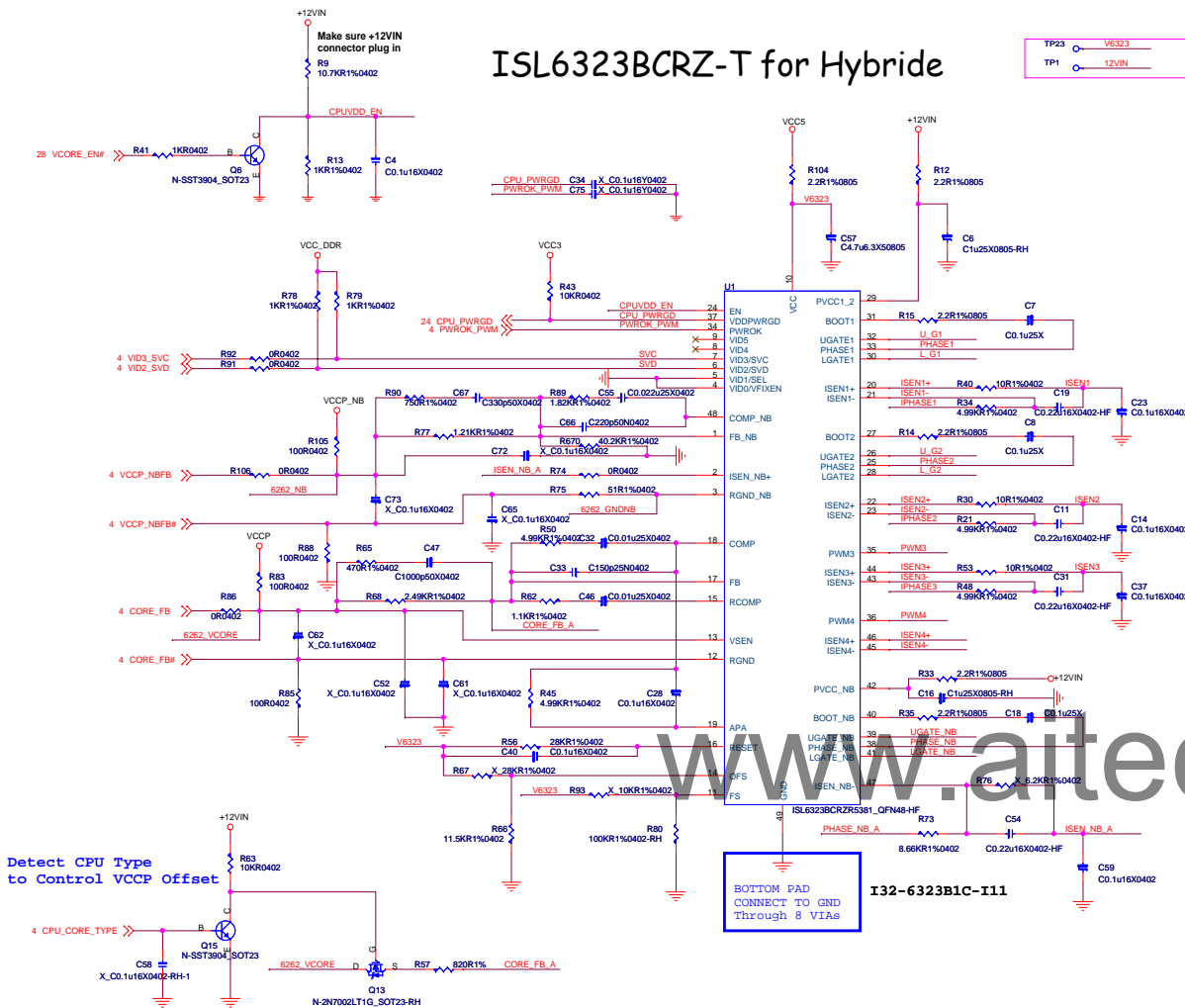
**MICRO-STAR INT'L CO.,LTD**

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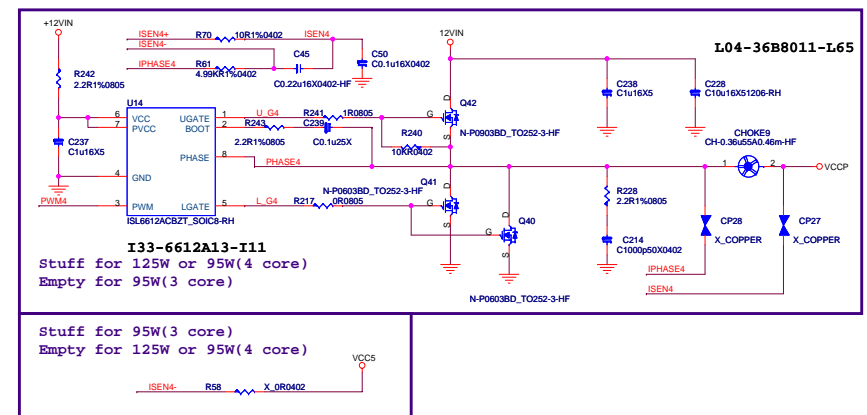
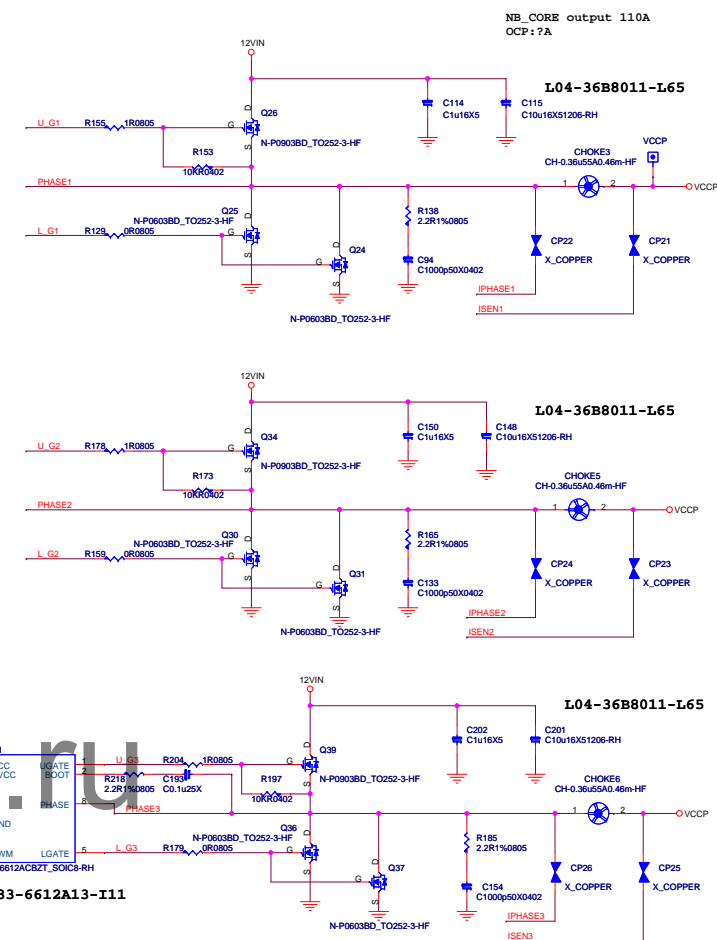
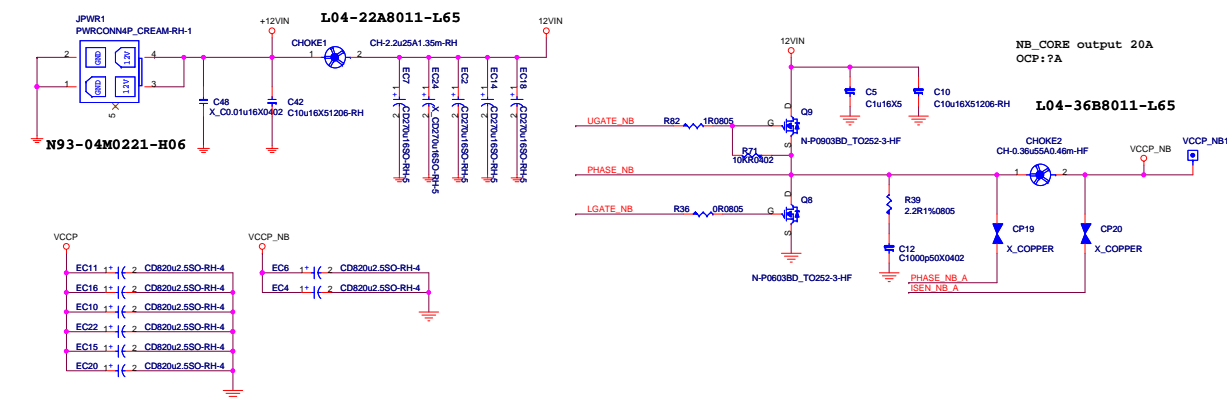
Size	Document Description
Custom	<b>ACPI Controller</b>

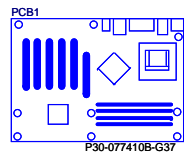
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## ISL6323BCRZ-T for Hybride

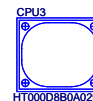
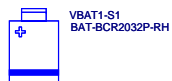


ATX Power Connector (2x4)



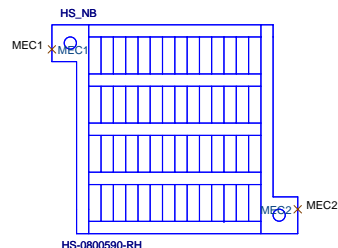
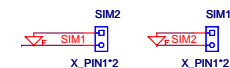


P30-077410B-G37  
P30-077410B-E55

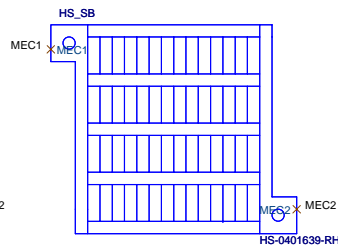


HT000D8B0A029  
E95-0000003-H06

### Simulation

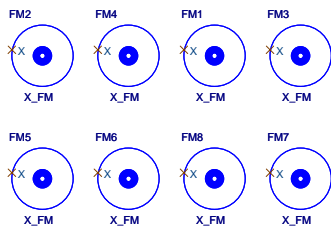


HS-0800590-RH  
E31-0800590-K08



HS-0401639-RH  
E31-0401639-K08

### Optics Orientation Holes



### Mounting Holes

